ADVANCE INFORMATION

80960HA/HD/HT

32-BIT HIGH-PERFORMANCE SUPERSCALAR PROCESSOR

- **32-Bit Parallel Architecture**
  - **Load/Store Architecture**
  - **Sixteen 32-Bit Global Registers**
  - **Sixteen 32-Bit Local Registers**
  - **1.2 Gbyte Internal Bandwidth (75 MHz)**
  - **On-Chip Register Cache**
- **Processor Core Clock**
  - **80960HA is 1x Bus Clock**
  - **80960HD is 2x Bus Clock**
  - **80960HT is 3x Bus Clock**
- **Binary Compatible with Other 80960 Processors**
- **Issue Up To 150 Million Instructions per Second**
- **High-Performance On-Chip Storage**
  - **16 Kbyte Four-Way Set-Associative Instruction Cache**
  - **8 Kbyte Four-Way Set-Associative Data Cache**
  - **2 Kbyte General Purpose RAM**
  - **Separate 128-Bit Internal Paths For Instructions/Data**
- **3.3V Supply Voltage**
  - **5V Tolerant Inputs**
  - **TTL Compatible Outputs**
- **Guarded Memory Unit**
  - **Provides Memory Protection**
  - **User/Supervisor Read/Write/Execute**
- **32-Bit Demultiplexed Burst Bus**
  - **Per-Byte Parity Generation/Checking**
  - **Address Pipelining Option**
  - **Fully Programmable Wait State Generator**
  - **Supports 8-, 16- or 32-Bit Bus Widths**
  - **160 Mbyte/s External Bandwidth (40 MHz)**
- **High-Speed Interrupt Controller**
  - **Up to 240 External Interrupts**
  - **31 Fully Programmable Priorities**
  - **Separate, Non-maskable Interrupt Pin**
- **Dual On-Chip 32-Bit Timers**
  - **Auto Reload Capability and One-Shot**
  - **CLKIN Prescaling, ÷1, 2, 4 or 8**
- **JTAG Support - IEEE 1149.1 Compliant**

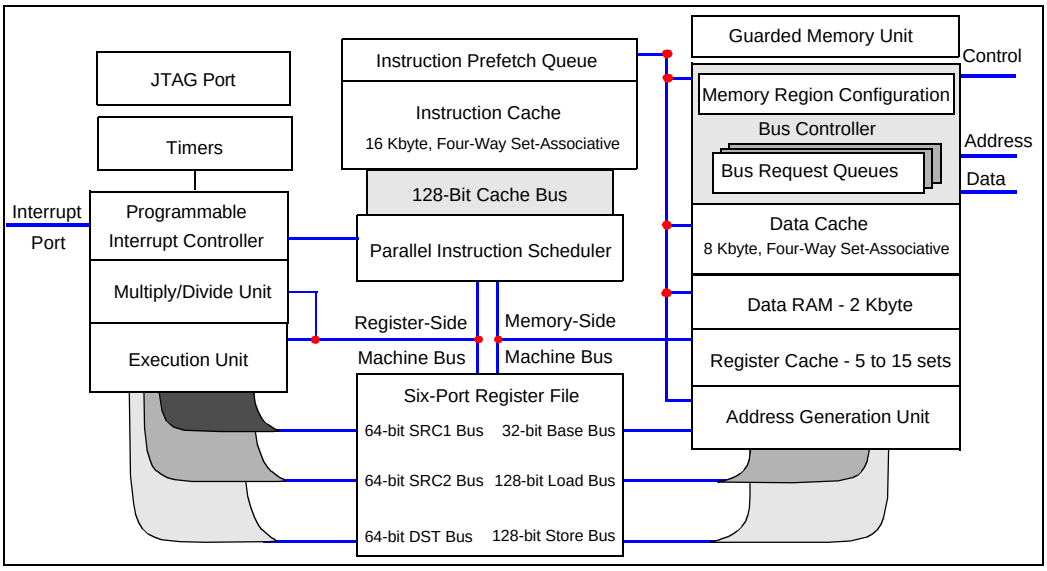


Figure 1. 80960Hx Block Diagram

May 1995 **Order Number: 272495-003**

80960HA/HD/HT
32-BIT HIGH-PERFORMANCE SUPERSCALAR PROCESSOR

ADVANCE INFORMATION

ADVANCE INFORMATION

1.0 ABOUT THIS DOCUMENT

This document provides a preview of Intel's 80960Hx embedded superscalar microprocessors. Future revisions of this document will provide targeted electrical characteristics. Detailed descriptions for functional topics — other than parametric performance — will be published in the *i960® Hx Microprocessor User's Guide* (272484).

In this document, "80960Hx" and "i960 Hx processor" refer to the products described in Table 1. Throughout this document, information that is specific to each is clearly indicated.

NOTE:

Intel retains the right to make changes to these specifications at any time. In particular, descriptions of features, timings, packaging, and pinouts do not imply a commitment to implement them. In fact, this specification does not imply a commitment by Intel to design, manufacture, or sell the product described herein.

2.0 INTEL'S 80960Hx PROCESSOR

Intel's 80960Hx processor provides new performance levels while maintaining backward compatibility (pin* and software) with the i960® CA/CF processors. This newest member of the family of i960 32-bit, RISC-style, embedded processors, allows customers to create scalable designs which meet multiple price and performance points. This is accomplished by providing processors that can run at the bus speed or faster using Intel's clock multiplying technology (see Table 1).The 80960Hx core is capable of issuing 150 million instructions per second, using a sophisticated instruction scheduler that allows the processor to sustain a throughput of two instructions every core clock with a peak performance of three instructions per clock. The 80960Hx-series comprises three processors, which differ in the ratio of core clock speed versus the external bus speed:

In addition to expanded clock frequency options, the 80960Hx provides essential enhancements for an emerging class of high-performance embedded applications. Features include a larger instruction cache, data cache and data RAM than any other 80960 processor to date. It also boasts a 32-bit demultiplexed and pipelined burst bus, fast interrupt mechanism, guarded memory unit, wait state generator, dual programmable timers, ONCE and IEEE 1149.1-compliant boundary scan test and debug support, and new instructions.

* Though not drop-in replaceable. Customers can design systems that accept either 80960Hx or Cx processors.

Table 1. 80960Hx Product Description

Product	Core	Voltage	Operating Frequency (bus/core)
80960HA	1x	3.3 V*	25/25, 33/33, 40/40
80960HD	2x	3.3 V*	16/32, 25/50, 33/66
80960HT	3x	3.3 V*	20/60, 25/75

NOTES: *Processor inputs are 5 V tolerant.

2.1 The i960 Processor Family

The i960 processor family is a 32-bit RISC architecture created by Intel to serve the needs of embedded applications. The embedded market includes applications as diverse as industrial automation, avionics, image processing, graphics and communications.

Because all members of the i960 processor family share a common core architecture, i960 applications are code compatible. Each new processor in the family adds its own special set of functions to the core to satisfy the needs of a specific application or range of applications in the embedded market.

2.2 Key 80960Hx Features

2.2.1 Execution Architecture

Independent instruction paths inside the processor allow multiple, out-of-sequence instruction execution per clock. Register and resource scoreboarding interlocks maintain the logical integrity of sequential instructions that are being executed in parallel. To sustain execution of multiple instructions in each clock cycle, the processor decodes multiple instructions in parallel and simultaneously issues these instructions to parallel processing units. The various

processing units are then able to independently access instruction operands in parallel from a common register set.

Local Register Cache integrated on-chip provides automatic register management on call/return instructions. Upon a call instruction, the processor allocates a set of local registers for the called procedure then stores the previous procedure's registers in the on-chip register cache. As additional procedures are called, the cache stores the associated registers such that the most recently called procedure is the first available by the next return (**ret**) instruction. The processor can store up to fifteen register sets, after which the oldest sets are stored (spilled) into external memory.

The 80960Hx supports the 80960 architecturally-defined branch prediction mechanism. This allows many branches to execute with no pipeline break. The 80960Hx's efficient pipeline results in a branch taking as few as zero clocks to execute. The maximum penalty for an incorrect prediction is two core clocks.

2.2.2 Pipelined, Burst Bus

A 32-bit high performance bus controller interfaces the 80960Hx core to the external memory and peripherals. The Bus Control Unit features a maximum transfer rate of 160 Mbytes per second (at a 40 MHz external bus clock frequency). One of the key advantages of this design is its versatility. The user can program system memory's physical and logical attributes independently. Physical attributes include wait state profile, bus width and parity. Logical attributes include cacheability and Big or Little Endian byte order. Internally programmable wait states and 16 separately configurable physical memory regions allow the processor to interface with a variety of memory subsystems with minimum system complexity. To reduce the effect of wait states, the bus design is decoupled from the core. This lets the processor execute instructions while the bus performs memory accesses independently.

The Bus Controller's key features include:

- Demultiplexed, Burst Bus to support most efficient DRAM access modes
- Address Pipelining to reduce memory cost while maintaining performance
- 32-, 16- and 8-bit modes for I/O interfacing ease
- Full internal wait state generation to reduce system cost
- Little and Big Endian support
- Unaligned Access support implemented in hardware
- Three-deep request queue to decouple the bus from the core
- Independent physical and logical address space characteristics

2.2.3 On-Chip Caches and Data RAM

As shown in Figure 1, the 80960Hx provides generous on-chip cache and storage features to decouple CPU execution from the external bus. The processor includes a 16 Kbyte instruction cache, an 8 Kbyte data cache and 2 Kbytes of Data RAM. The caches are organized as 4-way set associative. Stores that hit the data cache are written through to memory. The data cache performs write allocation on cache misses. A fifteen-set stack frame cache allows the processor to rapidly allocate and deallocate local registers. All of the on-chip RAM sustains a 4-word (128-bit) access every clock cycle.

2.2.4 Priority Interrupt Controller

The interrupt unit provides the mechanism for the low latency and high throughput interrupt service essential for embedded applications. A priority interrupt controller provides full programmability of 240 interrupt sources with a typical interrupt task switch (latency) time of 17 core clocks. The controller supports 31 priority levels. Interrupts are prioritized and signaled within 10 core clocks of the request. If the interrupt is a higher priority than the processor priority, the context switch to the interrupt routine typically completes in another 7 bus clocks.

External agents post interrupts via the 8-bit external interrupt port. The Interrupt unit also handles the two internal sources from the Timers. Interrupts can be level- or edge-triggered.

2.2.5 Guarded Memory Unit

The Guarded Memory Unit (GMU) provides memory protection without the address translation found in Memory Management Units. The GMU contains two memory protection schemes: one prevents illegal memory accesses, the other detects memory access violations. Both signal a fault to the processor. The programmable protection modes are: user read, write or execute; and supervisor read, write or execute.

2.2.6 Dual Programmable Timers

The processor provides two independent 32-bit timers, with four programmable clock rates. The user configures the timers via the Timer Unit registers. These registers are memory-mapped within the 80960Hx, addressable on 32-bit boundaries. The timers have a single-shot mode and auto-reload capabilities for continuous operation. Each timer has an independent interrupt request to the processor's interrupt controller.

2.2.7 Processor Self Test

When a system error is detected, the $\overline{\text{FAIL}}$ pin is asserted, a fail code message is driven onto the address bus, and the processor stops execution at the point of failure. The only way to resume normal operation is to perform a RESET operation. Because System Error generation can occur sometime after the bus confidence test and even after initialization during normal processor operation, the $\overline{\text{FAIL}}$ pin will be HIGH (logic "1") before the detection of a System Error.

The processor uses only one read bus-transaction to signal the fail code message; the address of the bus transaction is the fail code itself. The fail code is of the form: **0xfeffff***nn*; bits 6 to 0 contain a mask recording the possible failures. Bit 7, when set to 1, indicates the mask contains failures from the internal Built-In Self-Test (BIST); when 0, the mask indicates other failures.

Systems should ignore reserved bits 0 and 1. This is also true for bits 5 and 6, when bit 7 is clear (=0).

The mask is shown in Table 2 and Table 3.

Table 2. Fail Codes For BIST (bit 7 = 1)

Bit	When Set:
6	On-chip Data-RAM failure detected by BIST.
5	Internal Microcode ROM failure detected by BIST.
4	Instruction cache failure detected by BIST.
3	Data cache failure detected by BIST.
2	Local-register cache or processor core failure detected by BIST.
1	Reserved. Always zero.
0	Reserved. Always zero.

Table 3. Remaining Fail Codes (bit 7 = 0)

Bit	When Set:
6	Reserved. Always one.
5	Reserved. Always one.
4	A data structure within the IMI is not aligned to a word boundary.
3	A System Error during normal operation has occurred.
2	The Bus Confidence test has failed.
1	Reserved. Always zero.
0	Reserved. Always zero.

2.3 Instruction Set Summary

Table 4 summarizes the 80960Hx instruction set by logical groupings.

Table 4. 80960Hx Instruction Set

Data Movement	Arithmetic	Logical	Bit / Bit Field / Byte
Load	Add	And	Set Bit
Store	Subtract	Not And	Clear Bit
Move	Multiply	And Not	Not Bit
Load Address	Divide	Or	Alter Bit
Conditional Select[2]	Remainder	Exclusive Or	Scan For Bit
	Modulo	Not Or	Span Over Bit
	Shift	Or Not	Extract
	Extended Shift	Nor	Modify
	Extended Multiply	Exclusive Nor	Scan Byte for Equal
	Extended Divide	Not	Byte Swap[2]
	Add with Carry	Nand	
	Subtract with Carry		
	Rotate		
	Conditional Add[2]		
	Conditional Subtract[2]		
Comparison	**Branch**	**Call/Return**	**Fault**
Compare	Unconditional Branch	Call	Conditional Fault
Conditional Compare	Conditional Branch	Call Extended	Synchronize Faults
Compare and Increment	Compare and Branch	Call System	
Compare and Decrement		Return	
Compare byte[2]		Branch and Link	
Compare short[2]			
Test Condition Code			
Check Bit			
Debug	**Processor Mgmt**	**Atomic**	**Cache Control**
Modify Trace Controls	Flush Local Registers	Atomic Add	Instruction Cache Control[1,2]
Mark	Modify Arithmetic Controls	Atomic Modify	Data Cache Control[1,2]
Force Mark	Modify Process Controls		
	Interrupt Enable/ Disable[1,2]		
	System Control[1]		
	Halt[1,2]		

NOTES:
1) 80960Hx extensions to the 80960 core instruction set.
2) 80960Hx extensions to the 80960Cx instruction set

3.0 PACKAGE INFORMATION

This section describes the pins, pinouts and thermal characteristics for the 80960Hx in the 168-pin ceramic Pin Grid Array (PGA) package, 208-pin PowerQuad2* (PQ2). For complete package specifications and information, see the Intel *Packaging* Handbook (Order# 240800).

3.1 Pin Descriptions

This section defines the 80960Hx pins. Table 5 presents the legend for interpreting the pin descriptions in Table 6. All pins float while the processor is in the ONCE mode, except TDO, which can be driven active according to normal JTAG specifications.

Table 5. Pin Description Nomenclature

Symbol	Description
I	Input only pin.
O	Output only pin.
I/O	Pin can be input or output.
-	Pin must be connected as indicated for proper device functionality.
S(E)	Synchronous edge sensitive input. This input must meet the setup and hold times relative to CLKIN to ensure proper operation of the processor.
S(L)	Synchronous level sensitive input. This input must meet the setup and hold times relative to CLKIN to ensure proper operation of the processor.
A(E)	Asynchronous edge sensitive input.
A(L)	Asynchronous level sensitive input.
H(...)	While the processor bus is in the HOLD state (HLDA asserted), the pin: H(1) is driven to V_{CC} H(0) is driven to V_{SS} H(Z) floats H(Q) continues to be a valid output
B(...)	While the processor is in the bus backoff state ($\overline{BOFF}$ asserted), the pin: B(1) is driven to V_{CC} B(0) is driven to V_{SS} B(Z) floats B(Q) continues to be a valid output
R(...)	While the processor's $\overline{RESET}$ pin is asserted, the pin: R(1) is driven to V_{CC} R(0) is driven to V_{SS} R(Z) floats R(Q) continues to be a valid output
P(...)	While the processor is in HALT mode: P(1) is driven to V_{CC} P(0) is driven to V_{SS} P(Z) floats P(Q) continues to be a valid output

*PowerQuad is a trademark of Amkor Electronics.

Table 6. 80960Hx Processor Family Pin Descriptions (Sheet 1 of 5)

Name	Type	Description
A31:2	**O** H(Z) B(Z) R(Z) P(Q)	**ADDRESS BUS** carries the upper 30 bits of the physical address. A31 is the most significant address bit and A2 is the least significant. During a bus access, A31:2 identify all external addresses to word (4-byte) boundaries. The byte enable signals indicate the selected byte in each word. During burst accesses, A3 and A2 increment to indicate successive addresses.
D31:0	**I/O** S(L) H(Z) B(Z) R(Z) P(1)	**DATA BUS** carries 32, 16, or 8-bit data quantities depending on bus width configuration. The least significant bit of the data is carried on D0 and the most significant on D31. The lower 8 data lines (D7:0) are used when the bus is configured for 8-bit data. When configured for 16-bit data, D15:0 are used.
DP3:0	**I/O** S(L) H(Z) B(Z) R(Z) P(1)	**DATA PARITY** carries parity information for the data bus. Each parity bit is assigned a group of 8 data bus pins as follows: DP3 generates/checks parity for D31:24 DP2 generates/checks parity for D23:16 DP1 generates/checks parity for D15:8 DP0 generates/checks parity for D7:0 Parity information is generated for a processor write cycle and is checked for a processor read cycle. Parity checking and polarity are programmable. Parity generation/checking is only performed for the size of the data accessed.
$\overline{\text{PCHK}}$	**O** H(Q) B(Q) R(1) P(1)	**PARITY CHECK** indicates the result of parity check operation. When $\overline{\text{PCHK}}$ is asserted, the previous bus read access resulted in a parity check error.
$\overline{\text{BE3:0}}$	**O** H(Z) B(Z) R(1) P(1)	**BYTE ENABLES** select which of the four bytes addressed by A31:2 are active during a bus access. Byte enable encoding is dependent on the bus width of the memory region accessed: *32-bit bus:* $\overline{\text{BE3}}$ enables D31:24 $\overline{\text{BE2}}$ enables D23:16 $\overline{\text{BE1}}$ enables D15:8 $\overline{\text{BE0}}$ enables D7:0 *16-bit bus:* $\overline{\text{BE3}}$ becomes Byte High Enable (enables D15:8) $\overline{\text{BE2}}$ is not used (state is high) $\overline{\text{BE1}}$ becomes Address Bit 1 (A1) $\overline{\text{BE0}}$ becomes Byte Low Enable (enables D7:0) *8-bit bus:* $\overline{\text{BE3}}$ is not used (state is high) $\overline{\text{BE2}}$ is not used (state is high) $\overline{\text{BE1}}$ Address Bit 1 (A1) $\overline{\text{BE0}}$ Address Bit 0 (A0)

Table 6. 80960Hx Processor Family Pin Descriptions (Sheet 2 of 5)

Name	Type	Description
W/$\overline{R}$	**O** H(Z) B(Z) R(0) P(0)	**WRITE/READ** is low for read accesses and high for write accesses. W/$\overline{R}$ becomes valid during the address phase of a bus cycle and remains valid until the end of the cycle for non-pipelined accesses. For pipelined accesses, W/$\overline{R}$ changes state when the next address is presented. 0= Read 1= Write
D/$\overline{C}$	**O** H(Z) B(Z) R(0) P(0)	**DATA/CODE** indicates that a bus access is a data access or an instruction access. D/$\overline{C}$ has the same timing as W/$\overline{R}$. 0 = Code 1 = Data
$\overline{SUP}$	**O** H(Z) B(Z) R(1) P(Q)	**SUPERVISOR ACCESS** indicates whether the current bus access originates from a request issued while in supervisor mode or user mode. $\overline{SUP}$ can be used by the memory subsystem to isolate supervisor code and data structures from non-supervisor access. 0 = Supervisor Mode 1 = User Mode
$\overline{ADS}$	**O** H(Z) B(Z) R(1) P(1)	**ADDRESS STROBE** indicates a valid address and the start of a new bus access. $\overline{ADS}$ is asserted for the first clock of a bus access.
$\overline{READY}$	**I** S(L)	**$\overline{READY}$**, when enabled for a memory region, is asserted by the memory subsystem to indicate the completion of a data transfer. $\overline{READY}$ is used to indicate that read data on the bus is valid, or that a write transfer has completed. $\overline{READY}$ works in conjunction with the internal wait state generator to accommodate various memory speeds. $\overline{READY}$ is sampled after any programmed wait states: • During each data cycle of a burst access • During the data cycle of a non-burst access
$\overline{BTERM}$	**I** S(L)	**BURST TERMINATE**, when enabled for a memory region, is asserted by the memory subsystem to terminate a burst access in progress. When $\overline{BTERM}$ is asserted, the current burst access is terminated and another address cycle occurs.
$\overline{WAIT}$	**O** H(Z) B(Z) R(1) P(1)	**$\overline{WAIT}$** indicates the status of the internal wait-state generator. $\overline{WAIT}$ is asserted when the internal wait state generator generates N_{WAD}, N_{RAD}, N_{WDD} and N_{RDD} wait states. $\overline{WAIT}$ can be used to derive a write data strobe.
$\overline{BLAST}$	**O** H(Z) B(Z) R(1) P(1)	**BURST LAST** indicates the last transfer in a bus access. $\overline{BLAST}$ is asserted in the last data transfer of burst and non-burst accesses after the internal wait-state generator reaches zero. $\overline{BLAST}$ remains active as long as wait states are inserted via the $\overline{READY}$ pin. $\overline{BLAST}$ becomes inactive after the final data transfer in a bus cycle.

Table 6. 80960Hx Processor Family Pin Descriptions (Sheet 3 of 5)

Name	Type	Description
DT/$\overline{R}$	**O** H(Z) B(Z) R(0) P(0)	**DATA TRANSMIT/RECEIVE** indicates direction for data transceivers. DT/$\overline{R}$ is used with $\overline{DEN}$ to provide control for data transceivers connected to the data bus. DT/$\overline{R}$ is driven low to indicate the processor expects data (a read cycle). DT/$\overline{R}$ is driven high when the processor is “transmitting” data (a store cycle). DT/$\overline{R}$ only changes state when $\overline{DEN}$ is high. 0 = Data Receive 1 = Data Transmit
$\overline{DEN}$	**O** H(Z) B(Z) R(1) P(1)	**DATA ENABLE** indicates data transfer cycles during a bus access. $\overline{DEN}$ is asserted at the start of the first data cycle in a bus access and de-asserted at the end of the last data cycle. $\overline{DEN}$ is used with DT/$\overline{R}$ to provide control for data transceivers connected to the data bus. $\overline{DEN}$ remains asserted for sequential reads from pipelined memory regions.
$\overline{LOCK}$	**O** H(Z) B(Z) R(1) P(1)	**BUS LOCK** indicates that an atomic read-modify-write operation is in progress. $\overline{LOCK}$ may be used by the memory subsystem to prevent external agents from accessing memory which is currently involved in an atomic operation (e.g. a semaphore). $\overline{LOCK}$ is asserted in the first clock of an atomic operation and de-asserted when $\overline{BLAST}$ is deasserted in the last bus cycle.
HOLD	**I** S(L)	**HOLD REQUEST** signals that an external agent requests access to the processor’s address, data and control buses. When HOLD is asserted, the processor: • Completes the current bus request. • Asserts HOLDA and floats the address, data, and control buses. When HOLD is deasserted, the HOLDA pin is deasserted and the processor reassumes control of the address, data, and control pins.
HOLDA	**O** H(1) B(0) R(Q) P(Q)	**HOLD ACKNOWLEDGE** indicates to an external master that the processor has relinquished control of the bus. The processor grants HOLD requests and enters the HOLDA state while the $\overline{RESET}$ pin is asserted. HOLDA is never granted while $\overline{LOCK}$ is asserted.
$\overline{BOFF}$	**I** S(L)	**BUS BACKOFF** forces the processor to immediately relinquish control of the bus on the next clock cycle. When $\overline{READY}$/$\overline{BTERM}$ is enabled and: • When $\overline{BOFF}$ is asserted, the address, data, and control buses are floated on the next clock cycle and the current access is aborted. • When $\overline{BOFF}$ is deasserted, the processor resumes by regenerating the aborted bus access. See Figure 45, BOFF Functional Timing (pg. 60) for $\overline{BOFF}$ timing requirements.
BREQ	**O** H(Q) B(Q) R(0) P(0)	**BUS REQUEST** indicates that a bus request is pending in the bus controller, but the processor *is not stalled* pending the result of the bus operation. BREQ can be used with BSTALL to indicate to an external bus arbiter the processor’s bus ownership requirements.

Table 6. 80960Hx Processor Family Pin Descriptions (Sheet 4 of 5)

Name	Type	Description
BSTALL	**O** H(Q) B(Q) R(0) P(0)	**BUS STALL** indicates that the processor has stalled pending the result of a request in the bus controller. When BSTALL is asserted, the processor *must* regain bus ownership to continue processing (i.e., it can no longer execute strictly out of on-chip cache memory).
CT3:0	**O** H(Z) B(Z) R(Z) P(7)	**CYCLE TYPE** indicates the type of bus cycle currently being started or processor state. CT3:0 encoding follows: **Cycle Type** / **ADS** / **CT3:0** Program-initiated access using 8-bit bus / 0 / 0000 Program-initiated access using 16-bit bus / 0 / 0001 Program-initiated access using 32-bit bus / 0 / 0010 Event-initiated access using 8-bit bus / 0 / 0100 Event-initiated access using 16-bit bus / 0 / 0101 Event-initiated access using 32-bit bus / 0 / 0110 Reserved / 0 / 0X11 Reserved for future products / 0 / 1XXX Processor not halted, otherwise reserved / 1 / 0X00 Processor not halted, otherwise reserved / 1 / 0X01 Processor not halted, otherwise reserved / 1 / 0X10 Reserved / 1 / 0011 Processor in HALT mode / 1 / 0111 Reserved for future products / 1 / 1XXX
$\overline{\text{XINT7:0}}$	**I** A(E) A(L)	**EXTERNAL INTERRUPT** pins are used to request interrupt service. These pins can be configured in three modes: *Dedicated Mode:* Each pin is assigned a dedicated interrupt level. Dedicated inputs can be programmed to be level (low or high) or edge (rising or falling) sensitive. *Expanded Mode:* All eight pins act as a vectored interrupt source. The interrupt pins are level sensitive in this mode. *Mixed Mode:* The $\overline{\text{XINT7:5}}$ pins act as dedicated sources and the $\overline{\text{XINT4:0}}$ pins act as the five most significant bits of a vectored source. The least significant bits of the vectored source are set to “010” internally.
$\overline{\text{NMI}}$	**I** A(E)	**NON-MASKABLE INTERRUPT** causes a non-maskable interrupt event to occur. $\overline{\text{NMI}}$ is the highest priority interrupt source. $\overline{\text{NMI}}$ is falling edge triggered.
CLKIN	**I**	**CLOCK INPUT** provides the time base for the 80960Hx. All internal circuitry is synchronized to CLKIN. All input and output timings are specified relative to CLKIN. For the 80960HD, the 2x internal clock is derived by multiplying the CLKIN frequency by 2. For the 80960HT, the 3x internal clock is derived by multiplying the CLKIN frequency by 3.
$\overline{\text{RESET}}$	**I** A(L)	**$\overline{\text{RESET}}$** forces the device into reset. $\overline{\text{RESET}}$ causes all external and internal signals to return to their reset state (if defined). The rising edge of $\overline{\text{RESET}}$ starts the processor boot sequence.

Table 6. 80960Hx Processor Family Pin Descriptions (Sheet 5 of 5)

Name	Type	Description
STEST	**I** S(L)	**SELF TEST**, when asserted during the rising edge of RESET, causes the processor to execute its built in self-test.
FAIL	**O** H(Q) B(Q) R(0) P(1)	**FAIL** indicates a failure of the processor's built-in self-test performed during initialization. FAIL is asserted immediately out of reset and toggles during self-test to indicate the status of individual tests. If self-test passes, FAIL is de-asserted and the processor branches to the user's initialization code. Should self-test fail, the FAIL pin is asserted and the processor ceases execution.
ONCE	**I**	**On-Circuit Emulation** control: the processor samples this pin during reset. If it is asserted low at the end of reset, the processor enters ONCE mode. In ONCE mode, the processor stops all clocks and floats all output pins except the TDO pin. ONCE includes a nominal 80 kΩ internal pull-up resistor.
TCK	**I**	**TEST CLOCK** provides the clocking function for IEEE 1149.1 Boundary Scan testing.
TDI	**I**	**TEST DATA INPUT** is the serial input pin for IEEE 1149.1 Boundary Scan testing.
TDO	**O**	**TEST DATA OUTPUT** is the serial output pin for IEEE 1149.1 Boundary Scan testing. ONCE does not disable this pin.
TRST	**I**	**TEST RESET** asynchronously resets the Test Access Port (TAP) controller. TRST must be held low TBD clock cycles after power-up. One method is to tie TRST to the RESET pin through a 10 kΩ resistor. An alternative is to provide TRST with a separate power-on-reset circuit. TRST includes a nominal 80 kΩ internal pull-up resistor.
TMS	**I**	**TEST MODE SELECT** is sampled at the rising edge of TCK. TCK controls the sequence of TAP controller state changes for IEEE 1149.1 Boundary Scan testing. TMS includes a nominal 80 kΩ internal pull-up resistor.
VCC5	**I**	**5 V REFERENCE VOLTAGE** input is the reference voltage for the 5 V-tolerant I/O buffers. This signal should be connected to +5 V for use with inputs which exceed 3.3 V. If all inputs are from 3.3 V components, this pin should be connected to 3.3 V.
VCCPLL	**I**	**PLL VOLTAGE** is the +3.3 VDC analog input for the PLL.
VOLDET	**O**	**VOLTAGE DETECT** signal allows external system logic to distinguish between a 5 V 80960Cx processor and the 3.3 V 80960Hx processor. This signal is active low for a 3.3 V 80960Hx (it is high impedance for 5 V 80960Cx). This pin is available only on the PGA version. 0 = 80960Hx 1 = 80960Cx

3.2 80960Hx Mechanical Data

3.2.1 80960Hx PGA Pinout

Figure 2 depicts the complete 80960Hx PGA pinout as viewed from the top side of the component (i.e., pins facing down). Figure 3 shows the complete 80960Hx PGA pinout as viewed from the pin-side of the package (i.e., pins facing up). Table 8 lists the 80960Hx pin names with package location. See Section 4.3, Recommended Connections (pg. 27) for specifications and recommended connections.

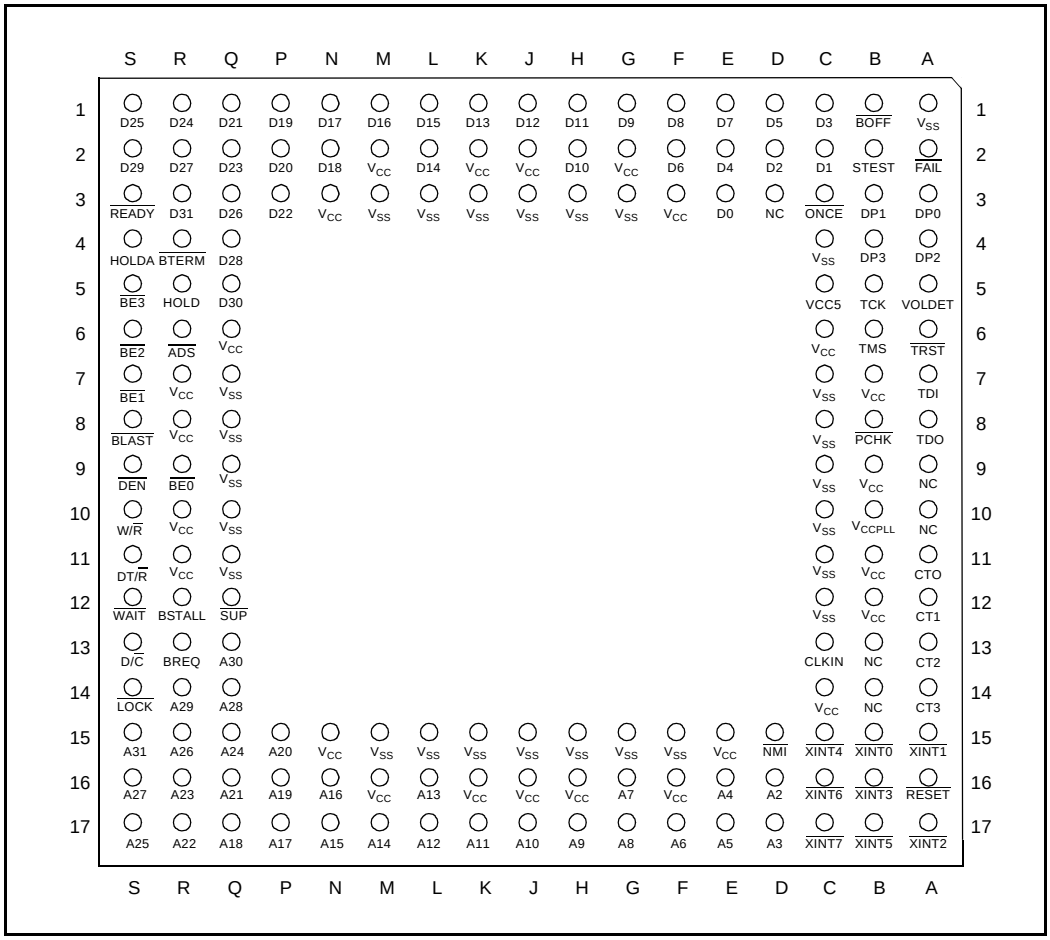


Figure 2. 80960Hx 168-Pin PGA Pinout — View from Top (Pins Facing Down)

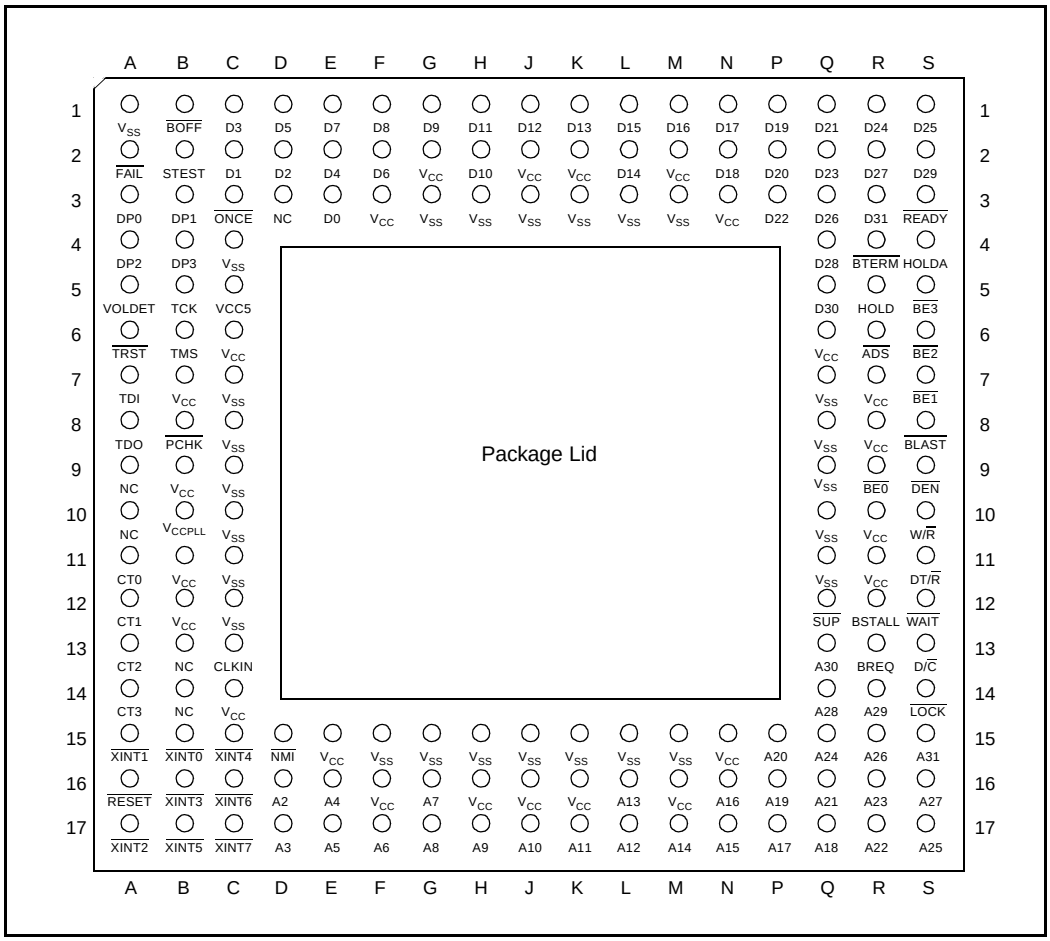


Figure 3. 80960Hx 168-Pin PGA Pinout — View from Bottom (Pins Facing Up)

Table 7. 80960Hx 168-Pin PGA Pinout — Signal Name Order (Sheet 1 of 2)

Signal Name	PGA Pin	Signal Name	PGA Pin	Signal Name	PGA Pin	Signal Name	PGA Pin
A2	D16	**$\overline{ADS}$**	R6	**D14**	L2	**$\overline{LOCK}$**	S14
A3	D17	**$\overline{BE0}$**	R9	**D15**	L1	**NC**	A9
A4	E16	**$\overline{BE1}$**	S7	**D16**	M1	**NC**	A10
A5	E17	**$\overline{BE2}$**	S6	**D17**	N1	**NC**	B13
A6	F17	**$\overline{BE3}$**	S5	**D18**	N2	**NC**	B14
A7	G16	**$\overline{BLAST}$**	S8	**D19**	P1	**NC**	D3
A8	G17	**$\overline{BOFF}$**	B1	**D20**	P2	**$\overline{NMI}$**	D15
A9	H17	**BREQ**	R13	**D21**	Q1	**$\overline{ONCE}$**	C3
A10	J17	**BSTALL**	R12	**D22**	P3	**$\overline{PCHK}$**	B8
A11	K17	**$\overline{BTERM}$**	R4	**D23**	Q2	**$\overline{READY}$**	S3
A12	L17	**CLKIN**	C13	**D24**	R1	**$\overline{RESET}$**	A16
A13	L16	**CT0**	A11	**D25**	S1	**STEST**	B2
A14	M17	**CT1**	A12	**D26**	Q3	**$\overline{SUP}$**	Q12
A15	N17	**CT2**	A13	**D27**	R2	**TCK**	B5
A16	N16	**CT3**	A14	**D28**	Q4	**TDI**	A7
A17	P17	**D/$\overline{C}$**	S13	**D29**	S2	**TDO**	A8
A18	Q17	**D0**	E3	**D30**	Q5	**TMS**	B6
A19	P16	**D1**	C2	**D31**	R3	**$\overline{TRST}$**	A6
A20	P15	**D2**	D2	**$\overline{DEN}$**	S9	**V_{CC}**	B7
A21	Q16	**D3**	C1	**DP0**	A3	**V_{CC}**	B9
A22	R17	**D4**	E2	**DP1**	B3	**V_{CC}**	B11
A23	R16	**D5**	D1	**DP2**	A4	**V_{CC}**	B12
A24	Q15	**D6**	F2	**DP3**	B4	**V_{CC}**	C6
A25	S17	**D7**	E1	**DT/$\overline{R}$**	S11	**V_{CC}**	C14
A26	R15	**D8**	F1	**$\overline{FAIL}$**	A2	**V_{CC}**	E15
A27	S16	**D9**	G1	**--**	--	**V_{CC}**	F3
A28	Q14	**D10**	H2	**--**	--	**V_{CC}**	F16
A29	R14	**D11**	H1	**--**	--	**V_{CC}**	G2
A30	Q13	**D12**	J1	**HOLD**	R5	**V_{CC}**	H16
A31	S15	**D13**	K1	**HOLDA**	S4	**V_{CC}**	J2

Table 7. 80960Hx 168-Pin PGA Pinout — Signal Name Order (Sheet 2 of 2)

Signal Name	PGA Pin	Signal Name	PGA Pin	Signal Name	PGA Pin	Signal Name	PGA Pin
V_{CC}	J16	V_{CCPLL}	B10	V_{SS}	H3	V_{SS}	Q10
V_{CC}	K2	**VOLDET**	A5	V_{SS}	H15	V_{SS}	Q11
V_{CC}	K16	V_{SS}	A1	V_{SS}	J3	**W/$\overline{R}$**	S10
V_{CC}	M2	V_{SS}	C4	V_{SS}	J15	**$\overline{WAIT}$**	S12
V_{CC}	M16	V_{SS}	C7	V_{SS}	K3	**$\overline{XINT0}$**	B15
V_{CC}	N3	V_{SS}	C8	V_{SS}	K15	**$\overline{XINT1}$**	A15
V_{CC}	N15	V_{SS}	C9	V_{SS}	L3	**$\overline{XINT2}$**	A17
V_{CC}	Q6	V_{SS}	C10	V_{SS}	L15	**$\overline{XINT3}$**	B16
V_{CC}	R7	V_{SS}	C11	V_{SS}	M3	**$\overline{XINT4}$**	C15
V_{CC}	R8	V_{SS}	C12	V_{SS}	M15	**$\overline{XINT5}$**	B17
V_{CC}	R10	V_{SS}	F15	V_{SS}	Q7	**$\overline{XINT6}$**	C16
V_{CC}	R11	V_{SS}	G3	V_{SS}	Q8	**$\overline{XINT7}$**	C17
V_{CC5}	C5	V_{SS}	G15	V_{SS}	Q9	**--**	--

Table 8. 80960Hx 168-pin PGA Pinout — Pin Number Order (Sheet 1 of 2)

PGA Pin	Signal Name	PGA Pin	Signal Name	PGA Pin	Signal Name	PGA Pin	Signal Name
A1	V_{SS}	**B14**	NC	**E15**	V_{CC}	**K15**	V_{SS}
A2	$\overline{FAIL}$	**B15**	$\overline{XINT0}$	**E16**	A4	**K16**	V_{CC}
A3	DP0	**B16**	$\overline{XINT3}$	**E17**	A5	**K17**	A11
A4	DP2	**B17**	$\overline{XINT5}$	**F1**	D8	**L1**	D15
A5	VOLDET	**C1**	D3	**F2**	D6	**L2**	D14
A6	$\overline{TRST}$	**C2**	D1	**F3**	V_{CC}	**L3**	V_{SS}
A7	TDI	**C3**	$\overline{ONCE}$	**F15**	V_{SS}	**L15**	V_{SS}
A8	TDO	**C4**	V_{SS}	**F16**	V_{CC}	**L16**	A13
A9	NC	**C5**	V_{CC5}	**F17**	A6	**L17**	A12
A10	NC	**C6**	V_{CC}	**G1**	D9	**M1**	D16
A11	CT0	**C7**	V_{SS}	**G2**	V_{CC}	**M2**	V_{CC}
A12	CT1	**C8**	V_{SS}	**G3**	V_{SS}	**M3**	V_{SS}
A13	CT2	**C9**	V_{SS}	**G15**	V_{SS}	**M15**	V_{SS}
A14	CT3	**C10**	V_{SS}	**G16**	A7	**M16**	V_{CC}
A15	$\overline{XINT1}$	**C11**	V_{SS}	**G17**	A8	**M17**	A14
A16	$\overline{RESET}$	**C12**	V_{SS}	**H1**	D11	**N1**	D17
A17	$\overline{XINT2}$	**C13**	CLKIN	**H2**	D10	**N2**	D18
B1	$\overline{BOFF}$	**C14**	V_{CC}	**H3**	V_{SS}	**N3**	V_{CC}
B2	STEST	**C15**	$\overline{XINT4}$	**H15**	V_{SS}	**N15**	V_{CC}
B3	DP1	**C16**	$\overline{XINT6}$	**H16**	V_{CC}	**N16**	A16
B4	DP3	**C17**	$\overline{XINT7}$	**H17**	A9	**N17**	A15
B5	TCK	**D1**	D5	**J1**	D12	**P1**	D19
B6	TMS	**D2**	D2	**J2**	V_{CC}	**P2**	D20
B7	V_{CC}	**D3**	NC	**J3**	V_{SS}	**P3**	D22
B8	$\overline{PCHK}$	**D15**	$\overline{NMI}$	**J15**	V_{SS}	**P15**	A20
B9	V_{CC}	**D16**	A2	**J16**	V_{CC}	**P16**	A19
B10	V_{CCPLL}	**D17**	A3	**J17**	A10	**P17**	A17
B11	V_{CC}	**E1**	D7	**K1**	D13	**Q1**	D21
B12	V_{CC}	**E2**	D4	**K2**	V_{CC}	**Q2**	D23
B13	NC	**E3**	D0	**K3**	V_{SS}	**Q3**	D26

Table 8. 80960Hx 168-pin PGA Pinout — Pin Number Order (Sheet 2 of 2)

PGA Pin	Signal Name	PGA Pin	Signal Name	PGA Pin	Signal Name	PGA Pin	Signal Name
Q4	D28	**Q16**	A21	**R11**	V_{CC}	**S6**	$\overline{BE2}$
Q5	D30	**Q17**	A18	**R12**	BSTALL	**S7**	$\overline{BE1}$
Q6	V_{CC}	**R1**	D24	**R13**	BREQ	**S8**	$\overline{BLAST}$
Q7	V_{SS}	**R2**	D27	**R14**	A29	**S9**	$\overline{DEN}$
Q8	V_{SS}	**R3**	D31	**R15**	A26	**S10**	W/$\overline{R}$
Q9	V_{SS}	**R4**	$\overline{BTERM}$	**R16**	A23	**S11**	DT/$\overline{R}$
Q10	V_{SS}	**R5**	HOLD	**R17**	A22	**S12**	$\overline{WAIT}$
Q11	V_{SS}	**R6**	$\overline{ADS}$	**S1**	D25	**S13**	D/$\overline{C}$
Q12	$\overline{SUP}$	**R7**	V_{CC}	**S2**	D29	**S14**	$\overline{LOCK}$
Q13	A30	**R8**	V_{CC}	**S3**	$\overline{READY}$	**S15**	A31
Q14	A28	**R9**	$\overline{BE0}$	**S4**	HOLDA	**S16**	A27
Q15	A24	**R10**	V_{CC}	**S5**	$\overline{BE3}$	**S17**	A25

3.2.2 80960Hx PQ2 Pinout

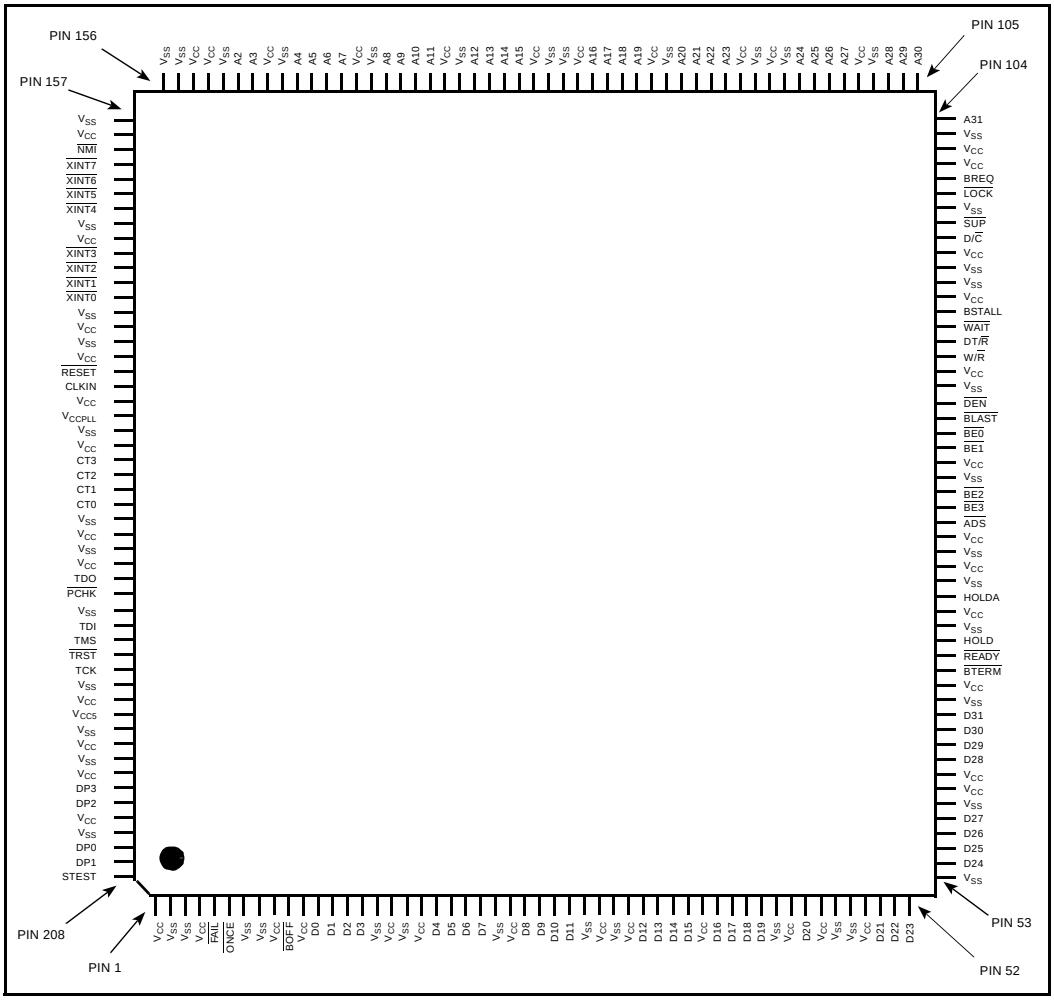


Figure 4. 80960Hx 208-Pin PQ2 Pinout

Table 9. 80960Hx PQ2 Pinout — Signal Name Order (Sheet 1 of 2)

Signal Name	PQ2 Pin	Signal Name	PQ2 Pin	Signal Name	PQ2 Pin	Signal Name	PQ2 Pin
A2	151	**$\overline{BE0}$**	83	**D16**	39	**$\overline{PCHK}$**	189
A3	150	**$\overline{BE1}$**	82	**D17**	40	**$\overline{READY}$**	68
A4	147	**$\overline{BE2}$**	79	**D18**	41	**$\overline{RESET}$**	174
A5	146	**$\overline{BE3}$**	78	**D19**	42	**STEST**	208
A6	145	**$\overline{BLAST}$**	84	**D20**	45	**$\overline{SUP}$**	97
A7	144	**$\overline{BOFF}$**	10	**D21**	50	**TCK**	194
A8	141	**BREQ**	100	**D22**	51	**TD0**	188
A9	140	**BSTALL**	91	**D23**	52	**TDI**	191
A10	139	**$\overline{BTERM}$**	67	**D24**	54	**TMS**	192
A11	138	**CLKIN**	175	**D25**	55	**$\overline{TRST}$**	193
A12	135	**CT0**	183	**D26**	56	**V_{CC}**	1
A13	134	**CT1**	182	**D27**	57	**V_{CC}**	4
A14	133	**CT2**	181	**D28**	61	**V_{CC}**	9
A15	132	**CT3**	180	**D29**	62	**V_{CC}**	11
A16	127	**D/$\overline{C}$**	96	**D30**	63	**V_{CC}**	17
A17	126	**D0**	12	**D31**	64	**V_{CC}**	19
A18	125	**D1**	13	**$\overline{DEN}$**	85	**V_{CC}**	25
A19	124	**D2**	14	**DP0**	206	**V_{CC}**	31
A20	121	**D3**	15	**DP1**	207	**V_{CC}**	33
A21	120	**D4**	20	**DP2**	203	**V_{CC}**	38
A22	119	**D5**	21	**DP3**	202	**V_{CC}**	44
A23	118	**D6**	22	**DT/$\overline{R}$**	89	**V_{CC}**	46
A24	113	**D7**	23	**$\overline{FAIL}$**	5	**V_{CC}**	49
A25	112	**D8**	26	**--**	**--**	**V_{CC}**	59
A26	111	**D9**	27	**--**	**--**	**V_{CC}**	60
A27	110	**D10**	28	**--**	**--**	**V_{CC}**	66
A28	107	**D11**	29	**HOLD**	69	**V_{CC}**	71
A29	106	**D12**	34	**HOLDA**	72	**V_{CC}**	74
A30	105	**D13**	35	**$\overline{LOCK}$**	99	**V_{CC}**	76
A31	104	**D14**	36	**$\overline{NMI}$**	159	**V_{CC}**	81
$\overline{ADS}$	77	**D15**	37	**$\overline{ONCE}$**	6	**V_{CC}**	87

Table 9. 80960Hx PQ2 Pinout — Signal Name Order (Sheet 2 of 2)

Signal Name	PQ2 Pin	Signal Name	PQ2 Pin	Signal Name	PQ2 Pin	Signal Name	PQ2 Pin
V_{CC}	92	V_{CC}	187	V_{SS}	70	V_{SS}	164
V_{CC}	95	V_{CC}	196	V_{SS}	73	V_{SS}	170
V_{CC}	101	V_{CC}	199	V_{SS}	75	V_{SS}	172
V_{CC}	102	V_{CC}	201	V_{SS}	80	V_{SS}	178
V_{CC}	109	V_{CC}	204	V_{SS}	86	V_{SS}	184
V_{CC}	115	V_{CC5}	197	V_{SS}	93	V_{SS}	186
V_{CC}	117	V_{CCPLL}	177	V_{SS}	94	V_{SS}	190
V_{CC}	123	V_{SS}	2	V_{SS}	98	V_{SS}	195
V_{CC}	128	V_{SS}	3	V_{SS}	103	V_{SS}	198
V_{CC}	131	V_{SS}	7	V_{SS}	108	V_{SS}	200
V_{CC}	137	V_{SS}	8	V_{SS}	114	V_{SS}	205
V_{CC}	143	V_{SS}	16	V_{SS}	116	**W/$\overline{R}$**	88
V_{CC}	149	V_{SS}	18	V_{SS}	122	**$\overline{WAIT}$**	90
V_{CC}	153	V_{SS}	24	V_{SS}	129	**$\overline{XINT0}$**	169
V_{CC}	154	V_{SS}	30	V_{SS}	130	**$\overline{XINT1}$**	168
V_{CC}	158	V_{SS}	32	V_{SS}	136	**$\overline{XINT2}$**	167
V_{CC}	165	V_{SS}	43	V_{SS}	142	**$\overline{XINT3}$**	166
V_{CC}	171	V_{SS}	47	V_{SS}	148	**$\overline{XINT4}$**	163
V_{CC}	173	V_{SS}	48	V_{SS}	152	**$\overline{XINT5}$**	162
V_{CC}	176	V_{SS}	53	V_{SS}	155	**$\overline{XINT6}$**	161
V_{CC}	179	V_{SS}	58	V_{SS}	156	**$\overline{XINT7}$**	160
V_{CC}	185	V_{SS}	65	V_{SS}	157	**--**	--

Table 10. 80960Hx PQ2 Pinout — Pin Number Order (Sheet 1 of 2)

PQ2 Pin	Signal Name	PQ2 Pin	Signal Name	PQ2 Pin	Signal Name	PQ2 Pin	Signal Name
1	V_{CC}	**31**	V_{CC}	**61**	D28	**91**	BSTALL
2	V_{SS}	**32**	V_{SS}	**62**	D29	**92**	V_{CC}
3	V_{SS}	**33**	V_{CC}	**63**	D30	**93**	V_{SS}
4	V_{CC}	**34**	D12	**64**	D31	**94**	V_{SS}
5	$\overline{FAIL}$	**35**	D13	**65**	V_{SS}	**95**	V_{CC}
6	$\overline{ONCE}$	**36**	D14	**66**	V_{CC}	**96**	D/$\overline{C}$
7	V_{SS}	**37**	D15	**67**	$\overline{BTERM}$	**97**	$\overline{SUP}$
8	V_{SS}	**38**	V_{CC}	**68**	$\overline{READY}$	**98**	V_{SS}
9	V_{CC}	**39**	D16	**69**	HOLD	**99**	$\overline{LOCK}$
10	$\overline{BOFF}$	**40**	D17	**70**	V_{SS}	**100**	BREQ
11	V_{CC}	**41**	D18	**71**	V_{CC}	**101**	V_{CC}
12	D0	**42**	D19	**72**	HOLDA	**102**	V_{CC}
13	D1	**43**	V_{SS}	**73**	V_{SS}	**103**	V_{SS}
14	D2	**44**	V_{CC}	**74**	V_{CC}	**104**	A31
15	D3	**45**	D20	**75**	V_{SS}	**105**	A30
16	V_{SS}	**46**	V_{CC}	**76**	V_{CC}	**106**	A29
17	V_{CC}	**47**	V_{SS}	**77**	$\overline{ADS}$	**107**	A28
18	V_{SS}	**48**	V_{SS}	**78**	$\overline{BE3}$	**108**	V_{SS}
19	V_{CC}	**49**	V_{CC}	**79**	$\overline{BE2}$	**109**	V_{CC}
20	D4	**50**	D21	**80**	V_{SS}	**110**	A27
21	D5	**51**	D22	**81**	V_{CC}	**111**	A26
22	D6	**52**	D23	**82**	$\overline{BE1}$	**112**	A25
23	D7	**53**	V_{SS}	**83**	$\overline{BE0}$	**113**	A24
24	V_{SS}	**54**	D24	**84**	$\overline{BLAST}$	**114**	V_{SS}
25	V_{CC}	**55**	D25	**85**	$\overline{DEN}$	**115**	V_{CC}
26	D8	**56**	D26	**86**	V_{SS}	**116**	V_{SS}
27	D9	**57**	D27	**87**	V_{CC}	**117**	V_{CC}
28	D10	**58**	V_{SS}	**88**	W/$\overline{R}$	**118**	A23
29	D11	**59**	V_{CC}	**89**	DT/$\overline{R}$	**119**	A22
30	V_{SS}	**60**	V_{CC}	**90**	$\overline{WAIT}$	**120**	A21

Table 10. 80960Hx PQ2 Pinout — Pin Number Order (Sheet 2 of 2)

PQ2 Pin	Signal Name	PQ2 Pin	Signal Name	PQ2 Pin	Signal Name	PQ2 Pin	Signal Name
121	A20	**143**	V_{CC}	**165**	V_{CC}	**187**	V_{CC}
122	V_{SS}	**144**	A7	**166**	$\overline{XINT3}$	**188**	TD0
123	V_{CC}	**145**	A6	**167**	$\overline{XINT2}$	**189**	$\overline{PCHK}$
124	A19	**146**	A5	**168**	$\overline{XINT1}$	**190**	V_{SS}
125	A18	**147**	A4	**169**	$\overline{XINT0}$	**191**	TDI
126	A17	**148**	V_{SS}	**170**	V_{SS}	**192**	TMS
127	A16	**149**	V_{CC}	**171**	V_{CC}	**193**	$\overline{TRST}$
128	V_{CC}	**150**	A3	**172**	V_{SS}	**194**	TCK
129	V_{SS}	**151**	A2	**173**	V_{CC}	**195**	V_{SS}
130	V_{SS}	**152**	V_{SS}	**174**	$\overline{RESET}$	**196**	V_{CC}
131	V_{CC}	**153**	V_{CC}	**175**	CLKIN	**197**	V_{CC5}
132	A15	**154**	V_{CC}	**176**	V_{CC}	**198**	V_{SS}
133	A14	**155**	V_{SS}	**177**	V_{CCPLL}	**199**	V_{CC}
134	A13	**156**	V_{SS}	**178**	V_{SS}	**200**	V_{SS}
135	A12	**157**	V_{SS}	**179**	V_{CC}	**201**	V_{CC}
136	V_{SS}	**158**	V_{CC}	**180**	CT3	**202**	DP3
137	V_{CC}	**159**	$\overline{NMI}$	**181**	CT2	**203**	DP2
138	A11	**160**	$\overline{XINT7}$	**182**	CT1	**204**	V_{CC}
139	A10	**161**	$\overline{XINT6}$	**183**	CT0	**205**	V_{SS}
140	A9	**162**	$\overline{XINT5}$	**184**	V_{SS}	**206**	DP0
141	A8	**163**	$\overline{XINT4}$	**185**	V_{CC}	**207**	DP1
142	V_{SS}	**164**	V_{SS}	**186**	V_{SS}	**208**	STEST

3.3 Package Thermal Specifications

The 80960Hx is specified for operation when T_C (case temperature) is within the range of 0^oC–85^oC. T_C may be measured in any environment to determine whether the 80960Hx is within the specified operating range. Measure the case temperature at the center of the top surface, opposite the pins. Refer to Figure 5.

T_A (ambient temperature) is calculated from θ_{CA} (thermal resistance from case to ambient) using the equation:

$T_A = T_C – P*\theta_{CA}$

Table 11 shows the maximum TA allowable (without exceeding T_C) at various airflows and operating frequencies (f_{CLKIN}).

Note that T_A is greatly improved by attaching fins or a heatsink to the package. P (maximum power consumption) is calculated by using the typical I_{CC} as tabulated in Section 4.5, DC Specifications (pg. 29) and V_{CC} of 3.3V.

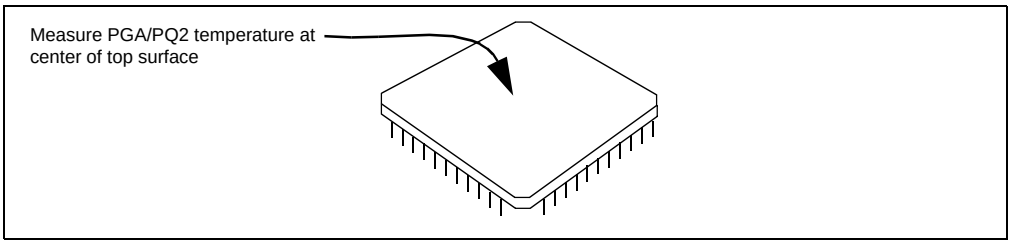


Figure 5. Measuring 80960Hx PGA Case Temperature

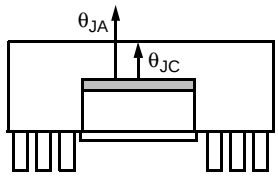
Table 11. Maximum T_A at Various Airflows in ^{O}C (PGA Package Only)

			Airflow-ft/min (m/sec)					
		f_{CLKIN} (MHz)	0 (0)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.06)	1000 (5.07)
Core 1X Bus Clock	T_A with Heatsink*	40	52.5	62.5	71.25	72.5	75.25	76.5
		33	59	67	74	75	77.2	78.2
		25	65.5	71.5	76.75	77.5	79.15	79.9
	T_A without Heatsink	40	42.5	50	57.5	62.5	67.25	68.5
		33	51	57	63	67	70.8	71.8
		25	59.5	64	68.5	71.5	74.35	75.1
Core 2X Bus Clock	T_A with Heatsink*	33	33	49	63	65	69.4	71.4
		25	46	58	68.5	70	73.3	74.8
	T_A without Heatsink	33	17	29	41	49	56.6	58.6
		25	34	43	52	58	63.7	65.2
Core 3X Bus Clock	T_A with Heatsink*	25	30	47	62	64	69	71
		20	33	49	63	65	69.4	71.4
	T_A without Heatsink	25	14	26	39	47	55	57
		20	17	29	41	49	56.6	58.6

NOTES: *0.285" high unidirectional heatsink (AI alloy 6061, 50 mil fin width, 150 mil center-to-center fin spacing).

Table 12. 80960Hx 168-Pin PGA Package Thermal Characteristics

Thermal Resistance — °C/Watt						
Parameter	Airflow — ft./min (m/sec)					
	0 (0)	200 (1.01)	400 (2.03)	600 (3.07)	800 (4.06)	1000 (5.07)
θ Junction-to-Case (Case measured as shown in Figure 5)	1.5	1.5	1.5	1.5	1.5	1.5
θ Case-to-Ambient (No Heatsink)	17	14	11	9	7.1	6.6
θ Case-to-Ambient (With Heatsink)*	13	9	5.5	5	3.9	3.4



NOTES:

1. This table applies to 80960Hx PGA plugged into socket or soldered directly to board.
2. $\theta_{JA} = \theta_{JC} + \theta_{CA}$

*0.285" high unidirectional heatsink (AI alloy 6061, 50 mil fin width, 150 mil center-to-center fin spacing).

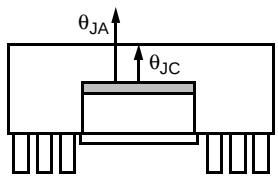
Table 13. Maximum T_A at Various Airflows in ^{O}C (PQ2 Package Only)

			Airflow-ft/min (m/sec)					
		f_{CLKIN} (MHz)	0 (0)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.06)	1000 (5.07)
Core 1X Bus Clock	T_A with Heatsink*	40	60.25	69.25	73.5	74.5	TBD	TBD
		33	65.2	72.4	75.8	76.6	TBD	TBD
		25	70.15	75.55	78.1	78.7	TBD	TBD
	T_A without Heatsink	40	57	62.25	66.5	66.75	TBD	TBD
		33	62.6	66.8	70.2	70.4	TBD	TBD
		25	68.2	71.35	73.9	74.05	TBD	TBD
Core 2X Bus Clock	T_A with Heatsink*	33	45.4	59.8	66.6	68.2	TBD	TBD
		25	55.3	66.1	71.2	72.4		
	T_A without Heatsink	33	40.2	48.6	55.4	55.8	TBD	TBD
		25	51.4	57.7	62.8	63.1	TBD	TBD
Core 3X Bus Clock	T_A with Heatsink*	25	43	59	66	67	TBD	TBD
		20	45.4	59.8	66.6	68.2	TBD	TBD
	T_A without Heatsink	25	38	47	54	54	TBD	TBD
		20	40.2	48.6	55.4	55.8	TBD	TBD

NOTES: *0.285" high unidirectional heatsink (AI alloy 6061, 50 mil fin width, 150 mil center-to-center fin spacing).

Table 14. 80960Hx 168-Pin PQ2 Package Thermal Characteristics

Thermal Resistance — °C/Watt						
Parameter	Airflow — ft./min (m/sec)					
	0 (0)	200 (1.01)	400 (2.03)	600 (3.07)	800 (4.06)	1000 (5.07)
θ Junction-to-Case (Case measured as shown in Figure 5)	1	1	1	1	1	1
θ Case-to-Ambient (No Heatsink)	11.2	9.1	7.4	7.3	TBD	TBD
θ Case-to-Ambient (With Heatsink)*	9.9	6.3	4.6	4.2	TBD	TBD



NOTES:

1. This table applies to 80960Hx PQ2 plugged into socket or soldered directly to board.
2. $\theta_{JA} = \theta_{JC} + \theta_{CA}$

*0.285" high unidirectional heatsink (AI alloy 6061, 50 mil fin width, 150 mil center-to-center fin spacing).

3.4 Heat Sink Adhesives

Intel recommends silicone-based adhesives to attach heat sinks to the PGA package. There is no particular recommendation concerning the PQ2 package.

3.5 PowerQuad2 Plastic Package

The 80960Hx family is available in an improved version of the common 208-lead SQFP plastic package called the PowerQuad2* (PQ2). The PQ2 package dimensions and lead pitch are identical to the SQFP package, so the PQ2 fits into the same board footprint. The advantage of the PQ2 package is the superior thermal conductivity that allows the plastic version of the 80960Hx to operate with the same 0 - 85°C temperature specifications as the more expensive ceramic PGA package.

The PQ2 package integrates a copper heat sink within the package to dissipate heat effectively. See Table 11 and Table 12 on page 23.

3.6 Stepping Register Information

The memory-mapped register at FF008710H contains the 80960Hx Device ID. The ID is identical to the ID obtained from a JTAG Query. Figure 6 defines the current 80960Hx Device IDs. The value for device identification is compliant with the IEEE 1149.1 specification and Intel standards. Table 15 describes the fields of the device ID.

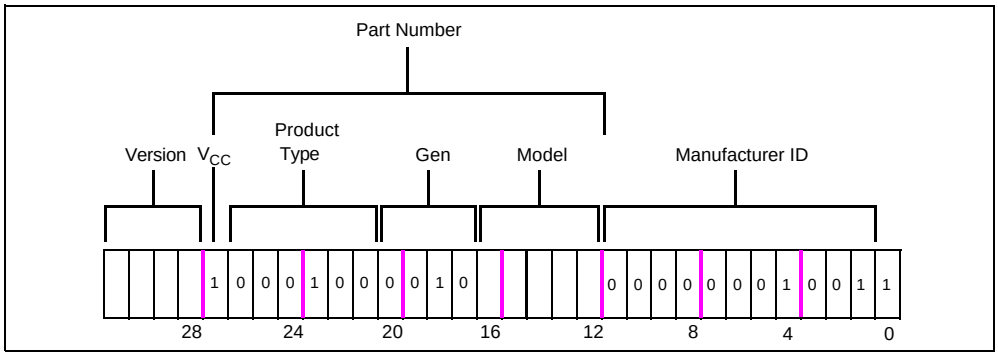


Figure 6. 80960Hx Device Identification Register

Table 15. Fields of 80960Hx Device ID

Field	Value	Definition
Version	0000 = A0 Step	Indicates major stepping changes.
V_{CC}	1 = 3.3 V device	Indicates a device is 3.3 V.
Product Type	00 0100 (Indicates i960 CPU)	Designates type of product.
Generation Type	0010 = H-series	Indicates the generation (or series) that the product belongs to.
Model	See Table 16	Indicates member within a series and specific model information.
Manufacturer ID	000 0000 1001 (Indicates Intel)	Manufacturer ID assigned by IEEE.

Table 16. 80960Hx Device ID Model Types

Device	Version	V_{CC}	Product	Gen.	Model	Manufacturer ID	'1'
80960HA	0000	1	000100	0010	00000	00000001001	1
80960HD	0000	1	000100	0010	00001	00000001001	1
80960HT	0000	1	000100	0010	00010	00000001001	1

3.7 Sources for Accessories

The following is a list of suggested sources for 80960Hx accessories. This is neither an endorsement nor a warranty of the performance of any of the listed products and/or companies.

Sockets

- 3M Textool Test and Interconnection Products
  6801 River Place Blvd. MS 130-3N-29
  Austin, TX 78726-2963
  (800) 328-0411 FAX: (800) 932-9372
- Augat, Inc. Interconnection Products Group
  452 John Dietsch Blvd. P.O. Box 2510
  Attleboro Falls, MA 02763
  (508) 699-7646
- Concept Mfg, Inc. (Decoupling Sockets)
  400 Walnut St. Suite 609
  Redwood City, CA 94063
  (415) 365-1162 FAX: (415) 365-1164

Heatsinks/Fins

- Thermalloy, Inc.
  2021 West Valley View Lane
  Dallas, TX 75234-8993
  (214) 243-4321 FAX: (214) 241-4656
- Wakefield Engineering, Inc.
  60 Audubon Road
  Wakefield, MA 01880
  (617) 245-5900 FAX: (617) 246-0874

4.0 ELECTRICAL SPECIFICATIONS

NOTICE: This document contains information on products in the design phase of development. Do not finalize a design with this information. Revised information will be published when the product is available.

4.1 Absolute Maximum Ratings

Parameter	Maximum Rating
Storage Temperature	–65°C to +150°C
Case Temperature Under Bias	–65°C to +110°C
Supply Voltage wrt. V_{SS}	–0.5V to + 4.6V
Voltage on V_{CC5} wrt. V_{SS}	–0.5V to + 6.5V
Voltage on Other Pins wrt. V_{SS}	–0.5V to V_{CC} + 0.5V

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

4.2 Operating Conditions

Table 17. Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage	3.0	3.6	V
V_{CC5}	Input Protection Bias	3.0	5.5	V
f_{CLKIN} 1xcore	Input Clock Frequency - 1x Core (80960HA)	16	40	MHz
f_{CLKIN} 2xcore	Input Clock Frequency - 2x Core (80960HD)	16	33	MHz
f_{CLKIN} 3xcore	Input Clock Frequency - 3x Core (80960HT)	16	25	MHz
T_C	Case Temp Under Bias PGA Pkg	0	85	°C

4.3 Recommended Connections

Power and ground connections must be made to multiple V_{CC} and V_{SS} (GND) pins. Every 80960Hx-based circuit board should include power (V_{CC}) and ground (V_{SS}) planes for power distribution. Every V_{CC} pin must be connected to the power plane; every V_{SS} pin must be connected to the ground plane. Pins identified as "NC" — no connect pins — **must not** be connected in the system.

Liberal decoupling capacitance should be placed near the 80960Hx. The processor can cause transient power surges when its numerous output buffers transition, particularly when connected to large capacitive loads.

Low inductance capacitors and interconnects are recommended for best high frequency electrical performance. Inductance can be reduced by shortening the board traces between the processor and decoupling capacitors as much as possible. Capacitors specifically designed for PGA packages will offer the lowest possible inductance.

For reliable operation, always connect unused inputs to an appropriate signal level. In particular, any unused interrupt ($\overline{XINT7:0}$, $\overline{NMI}$) input should be connected to V_{CC} through a pull-up resistor, as should $\overline{BTERM}$ if not used. Pull-up resistors should be in the in the range of 20 KΩ for each pin tied high. If $\overline{READY}$ or HOLD are not used, the unused input should be connected to ground. **N.C. pins must always remain unconnected.**

4.4 VCC5 Pin Requirements (V_{DIFF})

In mixed voltage systems that drive 80960Hx processor inputs in excess of 3.3V, the V_{CC5} pin must be connected to the system's 5V supply. To limit current flow into the V_{CC5} pin, there is a limit to the voltage differential between the V_{CC5} pin and the other V_{CC} pins. The voltage differential between the 80960Hx V_{CC5} pin and its 3.3V V_{CC} pins should never exceed 2.25V. This limit applies to power up, power down, and steady-state operation. Table 18 outlines this requirement.

Meeting this requirement ensures proper operation and guarantees that the current draw into the V_{CC5} pin does not exceed the I_{CC5} specification.

If the voltage difference requirements cannot be met due to system design limitations, an alternate solution may be employed. As shown in Figure 7, a minimum of 100 ohm series resistor may be used to limit the current into the V_{CC5} pin. This resistor ensures that current drawn by the V_{CC5} pin does not exceed the maximum rating for this pin.

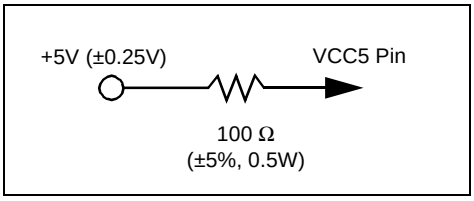


Figure 7. V_{CC5} Current-Limiting Resistor

This resistor is not necessary in systems that can guarantee the V_{DIFF} specification.

In 3.3V-only systems and systems that drive 80960Hx pins from 3.3V logic, connect the V_{CC5} pin directly to the 3.3V V_{CC} plane.

Table 18. V_{DIFF} Specification for Dual Power Supply Requirements (3.3V, 5V)

Symbol	Parameter	Min	Max	Units	Notes
V_{DIFF}	V_{CC5}-V_{CC} Difference		2.25	V	V_{CC5} input should not exceed V_{CC} by more than 2.25 V during power-up, power down or during steady-state operation.

4.5 DC Specifications

Table 19. DC Characteristics

Per the conditions described in Section 4.3, Recommended Connections (pg. 27).

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{IL}	Input Low Voltage	– 0.3		+0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC5} + 0.3	V	
V_{OL}	Output Low Voltage			0.4 0.2	V	I_{OL} = 3 mA I_{OL} = 100 µA
V_{OH}	Output High Voltage	2.4 V_{CC} – 0.2			V V	I_{OH} = –3 mA I_{OH} = – 100 µA
I_{LI}	Input Leakage Current Non-Test Inputs TDI, TMS, $\overline{TRST}$ and $\overline{ONCE}$ pins			 5 80	 µA µA	 $0 \le V_{IN} \le V_{CC}$ V_{IN} = 0V
I_{LO}	Output Leakage Current Non-Test Outputs TDO pin			 5 TBD	 µA µA	 $0.45 \le V_{OUT} \le V_{CC}$ TBD
I_{CC}	Operating Supply Current					
	80960HA		TBD	TBD	mA	(1,2)
	80960HD		TBD	TBD	mA	(1,2)
	80960HT		TBD	TBD	mA	(1,2)
I_{HALT}	HALT Mode Supply Current			TBD	mA	
I_{ONCE}	ONCE Mode Supply Current			TBD	mA	
C_{IN}	Input Capacitance for:					
	PQ2			TBD	pF	
	PGA			12	pF	F_C = 1 MHz
C_{OUT}	Output Capacitance of each output pin			12	pF	F_C = 1 MHz (3)
$C_{I/O}$	I/O Pin Capacitance			12	pF	F_C = 1 MHz
R_{PU}	Internal Pull-Up Resistance for TMS, TDI and $\overline{TRST}$	45	80	115	kΩ	

NOTES:

1. I_{CC} Maximum is measured at worst case frequency, V_{CC} and temperature, with device operating and outputs loaded to the test conditions described in Section 4.6.1, AC Test Conditions (pg. 32).
2. I_{CC} Typical is not tested.
3. Output Capacitance is the capacitive load of a floating output.

4.6 AC Specifications

Table 20. 80960Hx AC Characteristics (Sheet 1 of 2)

Per the conditions in Section 4.2, Operating Conditions (pg. 27) and Section 4.6.1, AC Test Conditions (pg. 32).

Symbol	Parameter		Min	Max	Units	Notes
Input Clock (1,7)						
TF	CLKIN Frequency	80960HA 80960HD 80960HT	16 16 16	40 33 25	MHz MHz MHz	
T	CLKIN Period	80960HA 80960HD 80960HT	25.0 30.3 40.0	62.5 62.5 62.5	ns ns ns	
TCS	CLKIN Period Stability			±0.1%	Δ	(11)
TCH	CLKIN High Time		8		ns	(11)
TCL	CLKIN Low Time	80960HA 80960HD 80960HT	8 8 8		ns ns ns	(11)
TCR	CLKIN Rise Time		0	4	ns	(11)
TCF	CLKIN Fall Time		0	4	ns	(11)
Synchronous Outputs (1,2,3,6)						
TOV1, TOH1	Output Valid Delay and Output Hold for all outputs except DT/$\overline{R}$ for 3.3V input signals. Same as above, but for 5.5V input signals.		1.5 1.5	10 13	ns ns	(13)
TOV2, TOH2	Output Valid Delay and Output Hold for DT/$\overline{R}$		T/2+1.5	T/2+10	ns	
TOF	Output Float for all outputs		1.5	9	ns	(11)
Synchronous Inputs (1,7,8,9)						
TIS	Input Setup		6.0		ns	
TIH	Input Hold		1.5		ns	
Relative Output Timings (1,2,3,6,10)						
TAVSH1	A31:2 Valid to $\overline{ADS}$ Rising		T – 4	T + 4	ns	(10)
TAVSH2	$\overline{BE3:0}$, W/$\overline{R}$, $\overline{SUP}$, D/$\overline{C}$, Valid to $\overline{ADS}$ Rising		T – 6	T + 6	ns	(10)
TAVEL1	A31:2 Valid to $\overline{DEN}$ Falling		T – 4	T + 4	ns	(10)
TAVEL2	$\overline{BE3:0}$, W/$\overline{R}$, $\overline{SUP}$, Valid to $\overline{DEN}$ Falling		T – 6	T + 6	ns	(10)
TNLQV	$\overline{WAIT}$ Falling to Output Data Valid		± 6		ns	(10)
TDVNH	Output Data Valid to $\overline{WAIT}$ Rising		N*T –6	N*T + 6	ns	(4), (10)
TNLNH	$\overline{WAIT}$ Falling to $\overline{WAIT}$ Rising		N*T ± 4		ns	(4), (10)
TNHQX	Output Data Hold after $\overline{WAIT}$ Rising		(N+1)*T–6	(N+1)*T+6	ns	(5), (10)

NOTES:
See Table 21, AC Characteristics Notes (pg. 31) for all notes related to AC specifications.

Table 20. 80960Hx AC Characteristics (Sheet 2 of 2)

Per the conditions in Section 4.2, Operating Conditions (pg. 27) and Section 4.6.1, AC Test Conditions (pg. 32).

Symbol	Parameter	Min	Max	Units	Notes
TEHTV	DT/$\overline{R}$ Hold after $\overline{DEN}$ High	T/2 – 7	∞	ns	(10)
TTVEL	DT/$\overline{R}$ Valid to $\overline{DEN}$ Falling	T/2 – 4		ns	(10)
Relative Input Timings (1,7,10)					
TIS7	$\overline{XINT7:0}$, $\overline{NMI}$ Input Setup	7		ns	(9)
TIH7	$\overline{XINT7:0}$, $\overline{NMI}$ Input Hold	3		ns	(9)
TIS8	$\overline{RESET}$ Input Setup	3		ns	(8)
TIH8	$\overline{RESET}$ Input Hold	T/4 + 1		ns	(8)

NOTES:
See Table 21, AC Characteristics Notes (pg. 31) for all notes related to AC specifications.

Table 21. AC Characteristics Notes

NOTES:

1. See Section 4.6.2, AC Timing Waveforms (pg. 32) for waveforms and definitions.
2. See Figure 24, Output Delay or Hold vs. Load Capacitance (pg. 39) for capacitive derating information for output delays and hold times.
3. See Figure 22, Rise and Fall Time Derating at 85oC and Minimum VCC (pg. 38) for capacitive derating information for rise and fall times.
4. Where N is the number of N_{RAD}, N_{RDD}, N_{WAD} or N_{WDD} wait states that are programmed in the Bus Controller Region Table. $\overline{WAIT}$ never goes active when there are no wait states in an access.
5. N = Number of wait states inserted with $\overline{READY}$.
6. These specifications are guaranteed by the processor.
7. These specifications must be met by the system for proper operation of the processor.
8. $\overline{RESET}$ is an asynchronous input which has no required setup and hold time for proper operation. However, to guarantee the device exits the reset mode synchronized to a particular clock edge, the rising edge of $\overline{RESET}$ must meet setup and hold times to the rising edge of the CLKIN.
9. The interrupt pins are synchronized internally by the 80960Hx. They have no required setup or hold times for proper operation. These pins are sampled by the interrupt controller every clock and must be active for at least two consecutive CLKIN rising edges when asserting them asynchronously. To guarantee recognition at a particular clock edge, the setup and hold times shown must be met.
10. Relative Output timings are not tested.
11. Not tested.
12. The processor minimizes changes to the bus signals when transitioning from a bus cycle to an idle bus for the following signals: A31:4, SUP, CT3:0, D/$\overline{C}$, $\overline{LOCK}$, W/$\overline{R}$, BE3:0.
13. Worst-case T_{OV} condition occurs on I/O pins when pins transition from a floating high input to driving a low output state. The Data Bus pins encounter this condition during a read followed by a write. 5 V signals take 3 ns longer to discharge than 3.3V signals at 50 pF loads.

Table 22. 80960Hx Boundary Scan Test Signal Timings

Symbol	Parameter	Min	Max	Units	Notes
T_{BSF}	TCK Frequency		8	MHz	
T_{BSC}	TCK Period	125		ns	
T_{BSCH}	TCK High Time	40		ns	Measured at 1.5 V (1)
T_{BSCL}	TCK Low Time	40		ns	Measured at 1.5 V (1)
T_{BSCR}	TCK Rise Time		8	ns	0.8 V to 2.0 V (1)
T_{BSCF}	TCK Fall Time		8	ns	2.0 V to 0.8 V (1)
T_{BSIS1}	Input Setup to TCK — TDI, TMS	8		ns	
T_{BSIH1}	Input Hold from TCK — TDI, TMS	10		ns	
T_{BSOV1}	TDO Valid Delay	3	30	ns	
T_{BSOF1}	TDO Float Delay		36	ns	(1)
T_{BSOV2}	All Outputs (Non-Test) Valid Delay	3	30	ns	Relative to TCK
T_{BSOF2}	All Outputs (Non-Test) Float Delay		36	ns	Relative to TCK (1)
T_{BSIS2}	Input Setup to TCK - All Inputs (Non-Test)	8		ns	
T_{BSIH2}	Input Hold from TCK - All Inputs (Non-Test)	10		ns	

NOTES:

1. Not tested.

4.6.1 AC Test Conditions

AC values are derived using the 50 pF load shown in Figure 8. Figure 9 shows how timings vary with load capacitance. Input waveforms (except for CLKIN) are assumed to have a rise and fall time of ≤ 2 ns from 0.8 V to 2.0 V.

4.6.2 AC Timing Waveforms

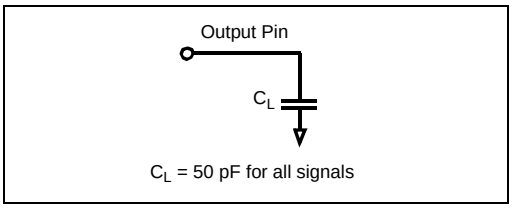


Figure 8. AC Test Load

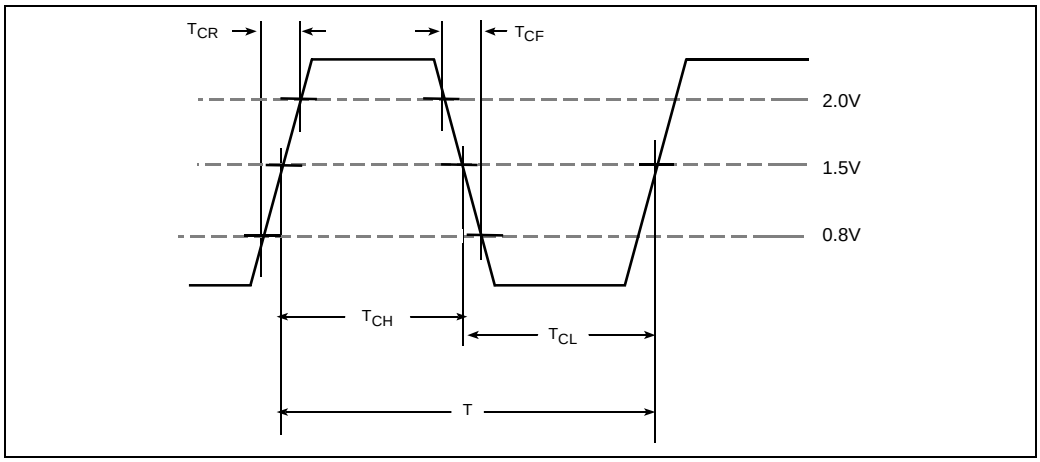


Figure 9. CLKIN Waveform

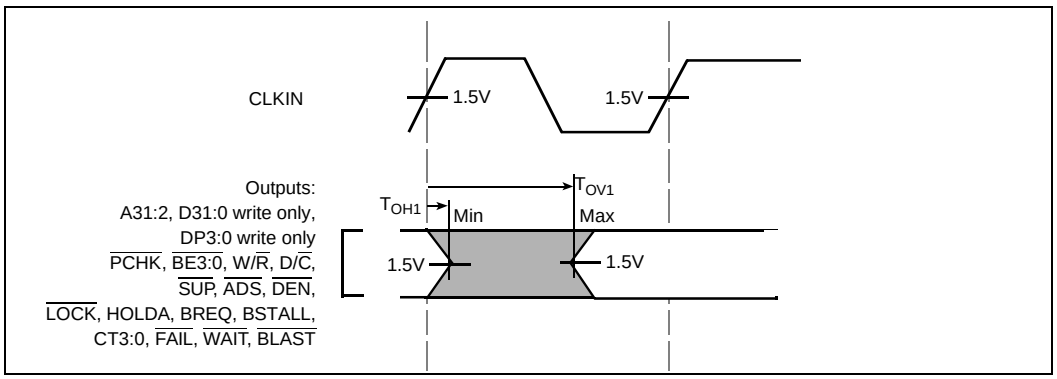


Figure 10. Output Delay Waveform

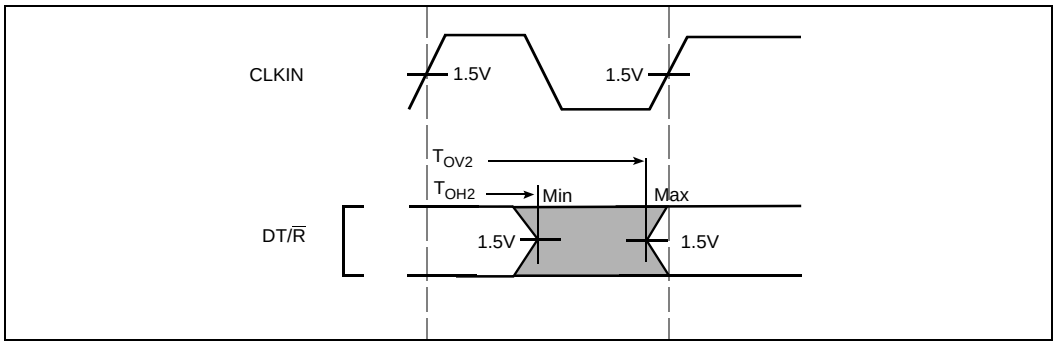


Figure 11. Output Delay Waveform

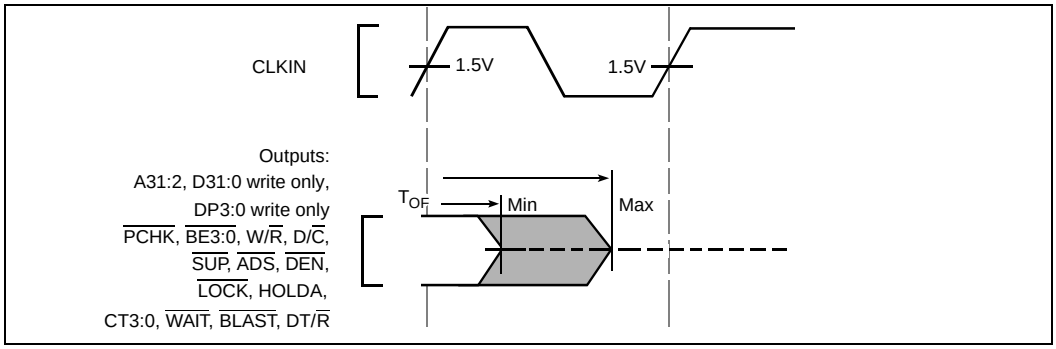


Figure 12. Output Float Waveform

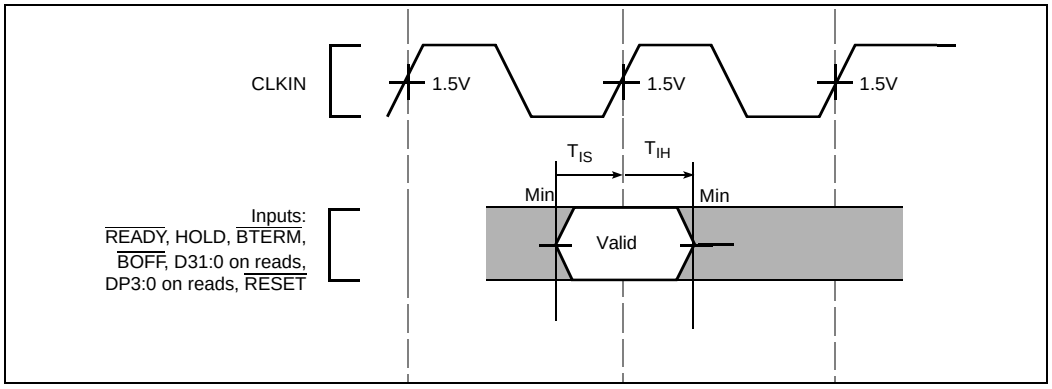
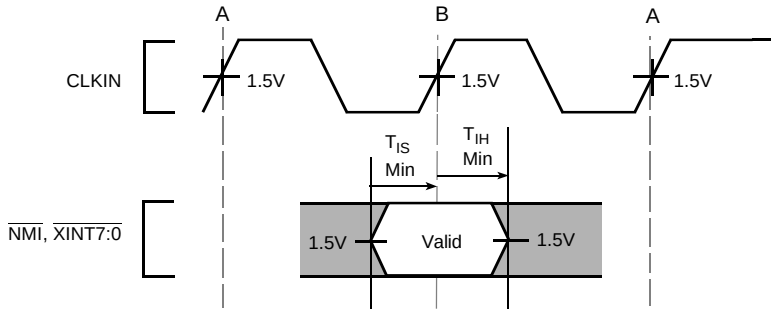
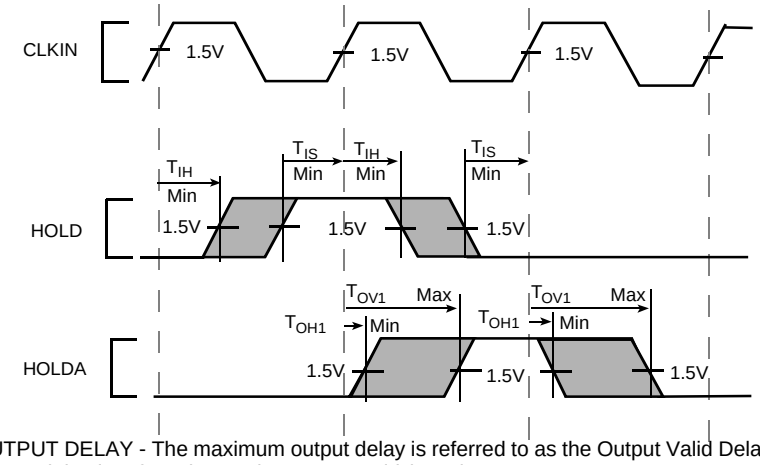


Figure 13. Input Setup and Hold Waveform



NOTE: A and B edges are established by de-assertion of RESET. See Figure 25, Cold Reset Waveform (pg. 40).

Figure 14. NMI, XINT7:0 Input Setup and Hold Waveform



T_{OV1} T_{OH1} — OUTPUT DELAY - The maximum output delay is referred to as the Output Valid Delay (T_{OV1}). The minimum output delay is referred to as the Output Hold (T_{OH1}).

T_{IS} T_{IH} — INPUT SETUP AND HOLD - The input setup and hold requirements specify the sampling window during which synchronous inputs must be stable for correct processor operation.

Figure 15. Hold Acknowledge Timings

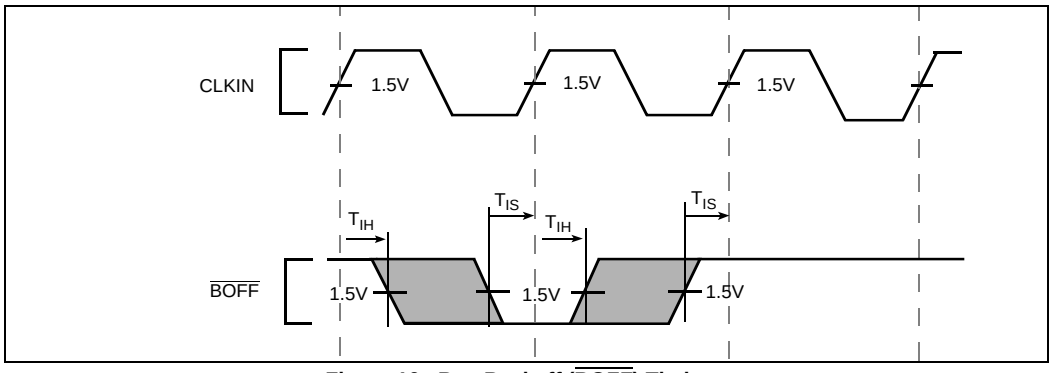


Figure 16. Bus Backoff ($\overline{BOFF}$) Timings

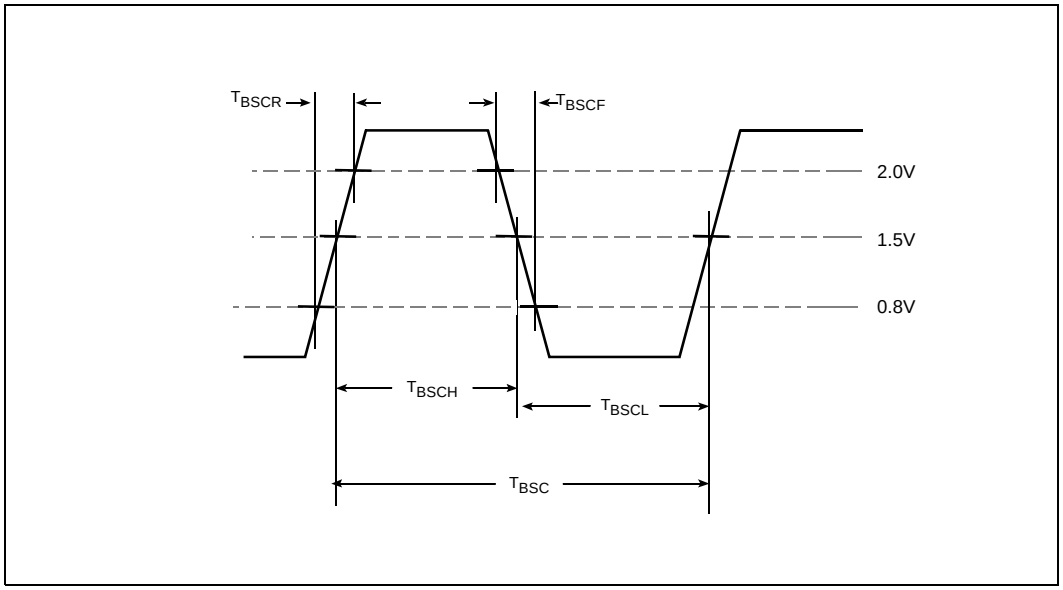


Figure 17. TCK Waveform

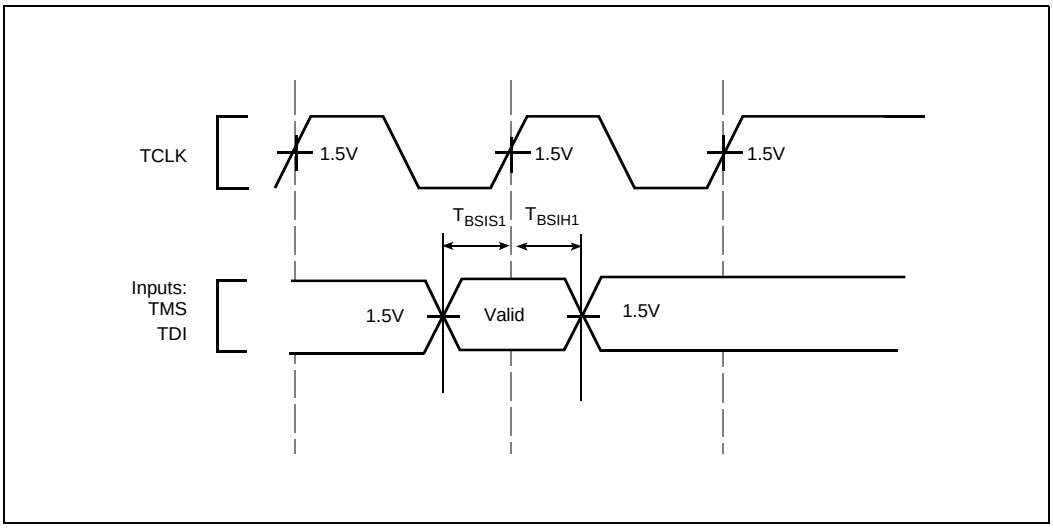


Figure 18. Input Setup and Hold Waveforms for T_{BSIS1} and T_{BSIH1}

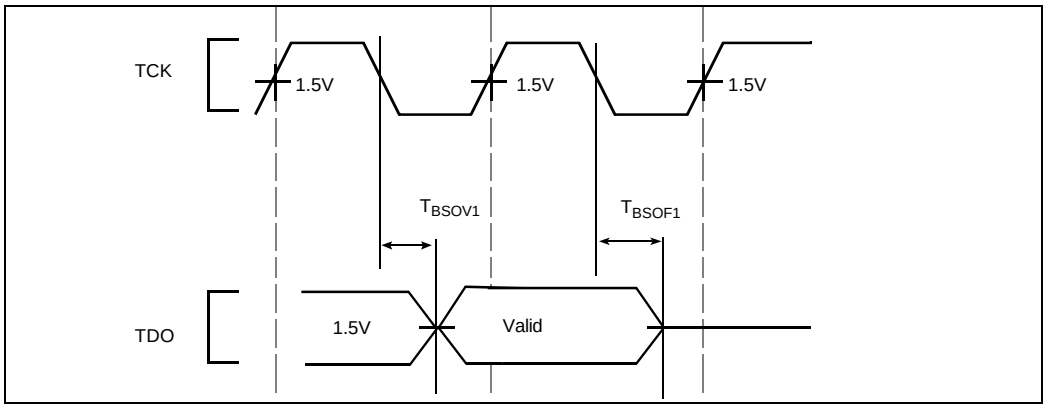


Figure 19. Output Delay and Output Float for T_{BSOV1} and T_{BSOF1}

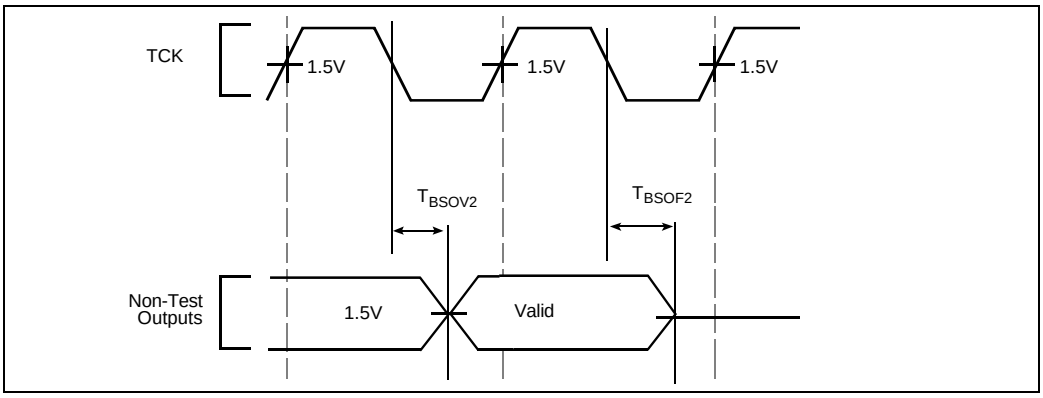


Figure 20. Output Delay and Output Float Waveform for T_{BSOV2} and T_{BSOF2}

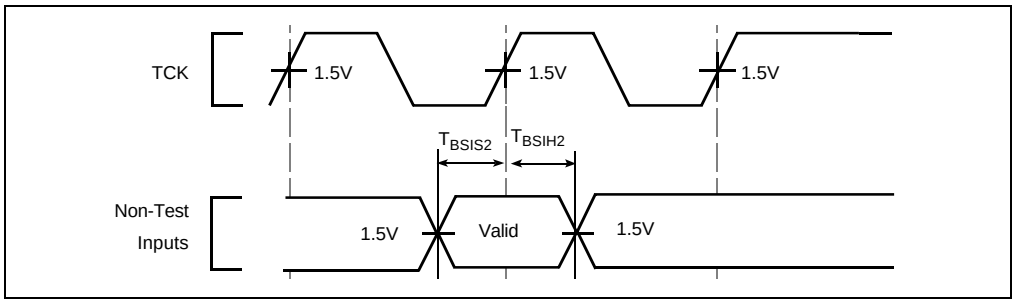


Figure 21. Input Setup and Hold Waveform for T_{BSIS2} and T_{BSIH2}

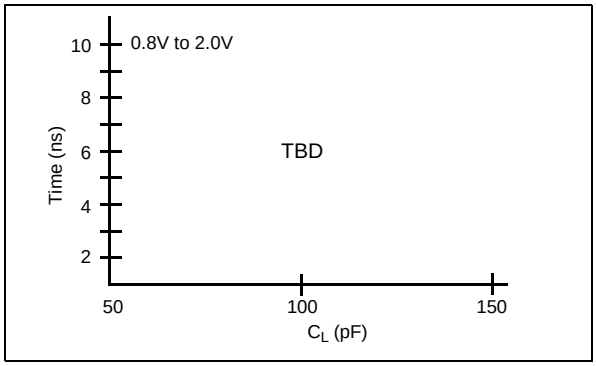


Figure 22. Rise and Fall Time Derating at 85°C and Minimum V_{CC}

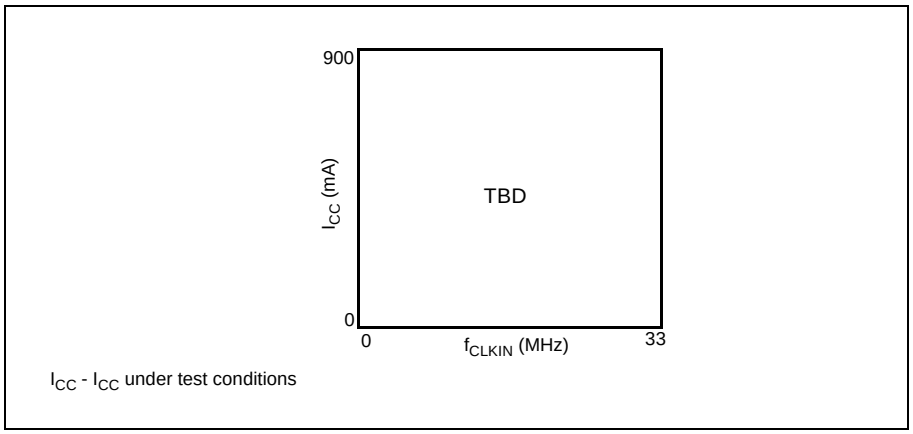


Figure 23. I_{CC} vs. Frequency and Temperature

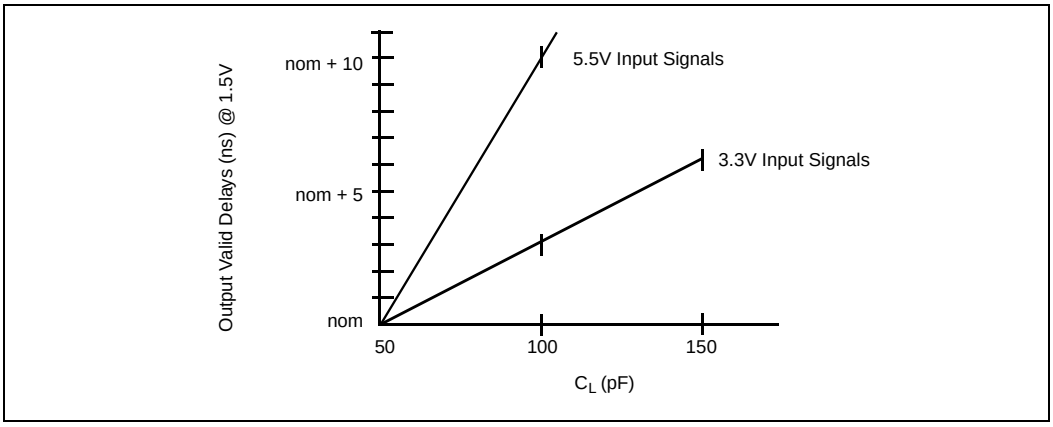


Figure 24. Output Delay or Hold vs. Load Capacitance

5.0 BUS WAVEFORMS

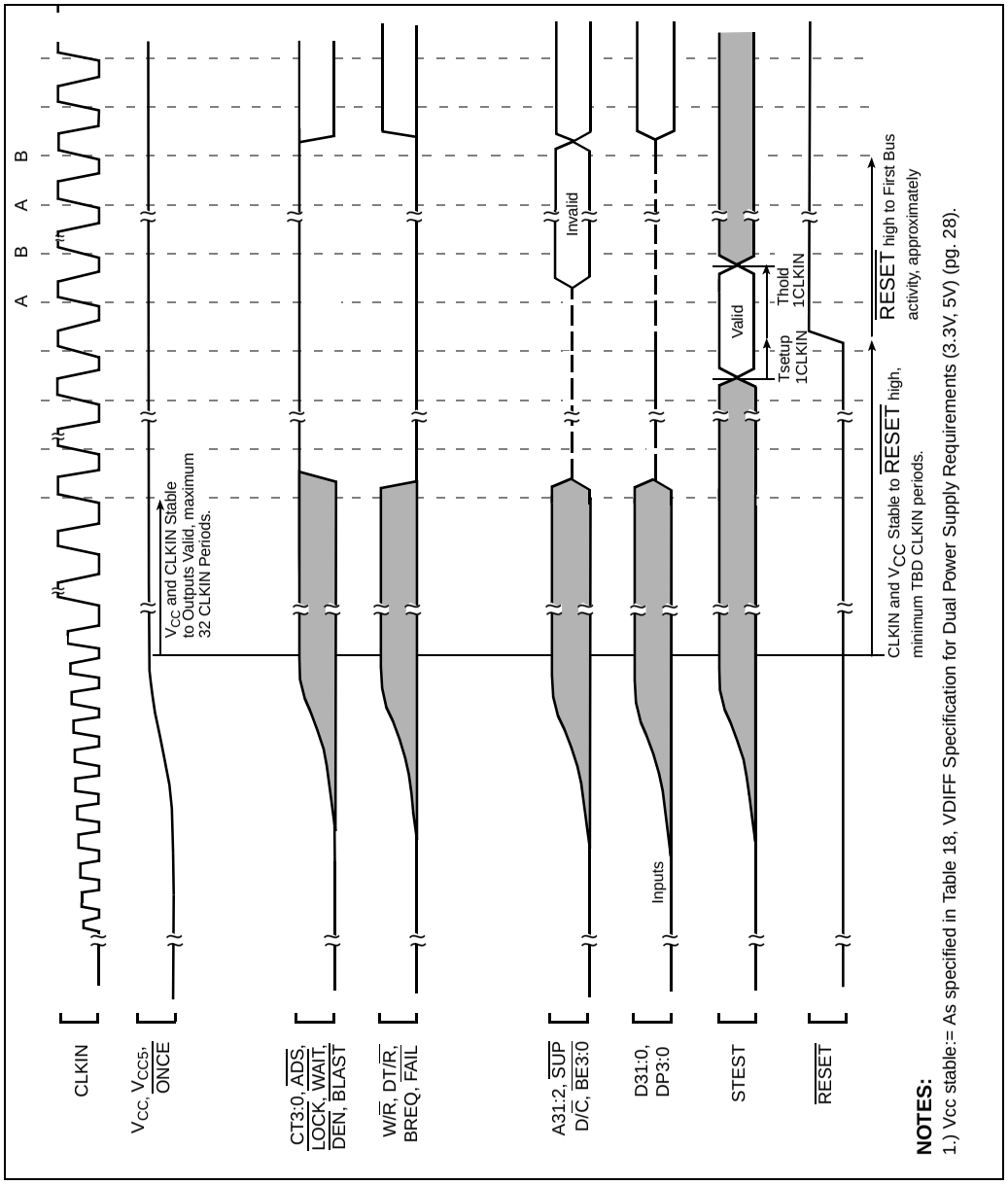


Figure 25. Cold Reset Waveform

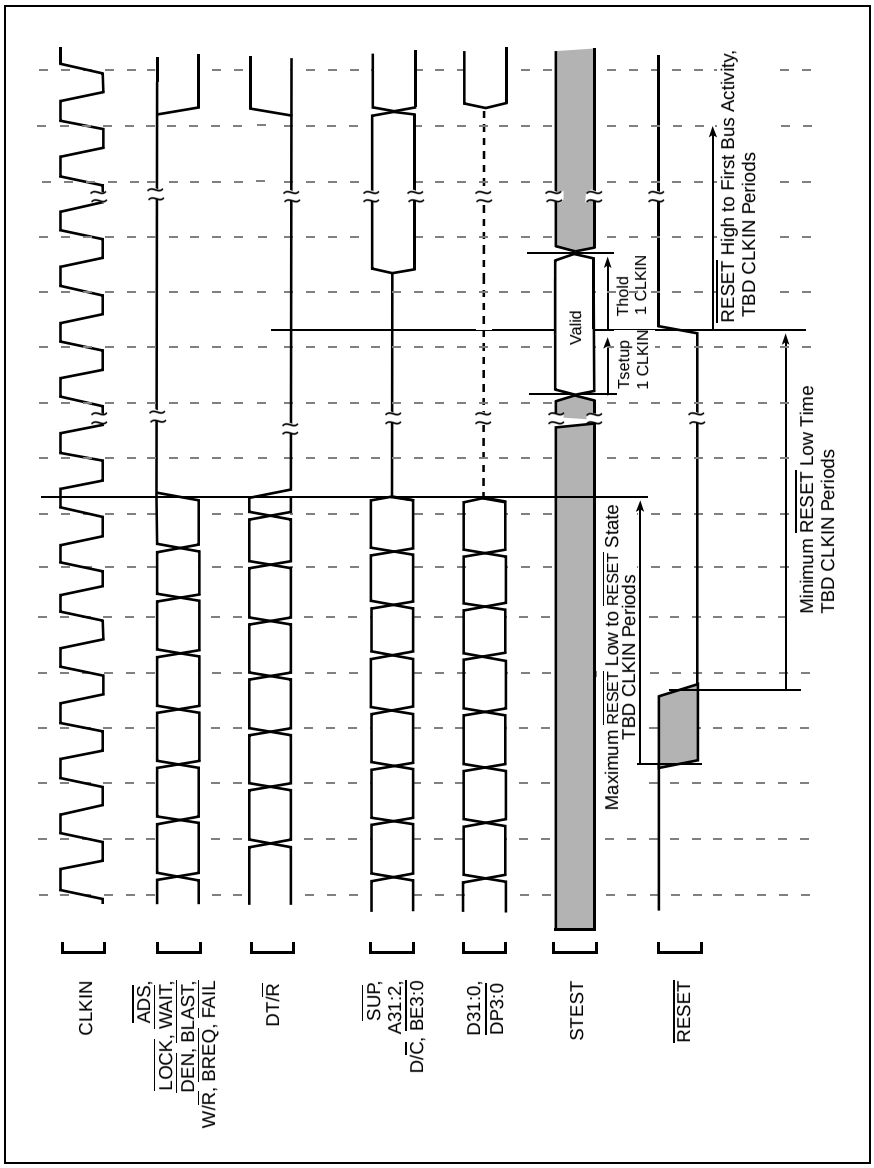


Figure 26. Warm Reset Waveform

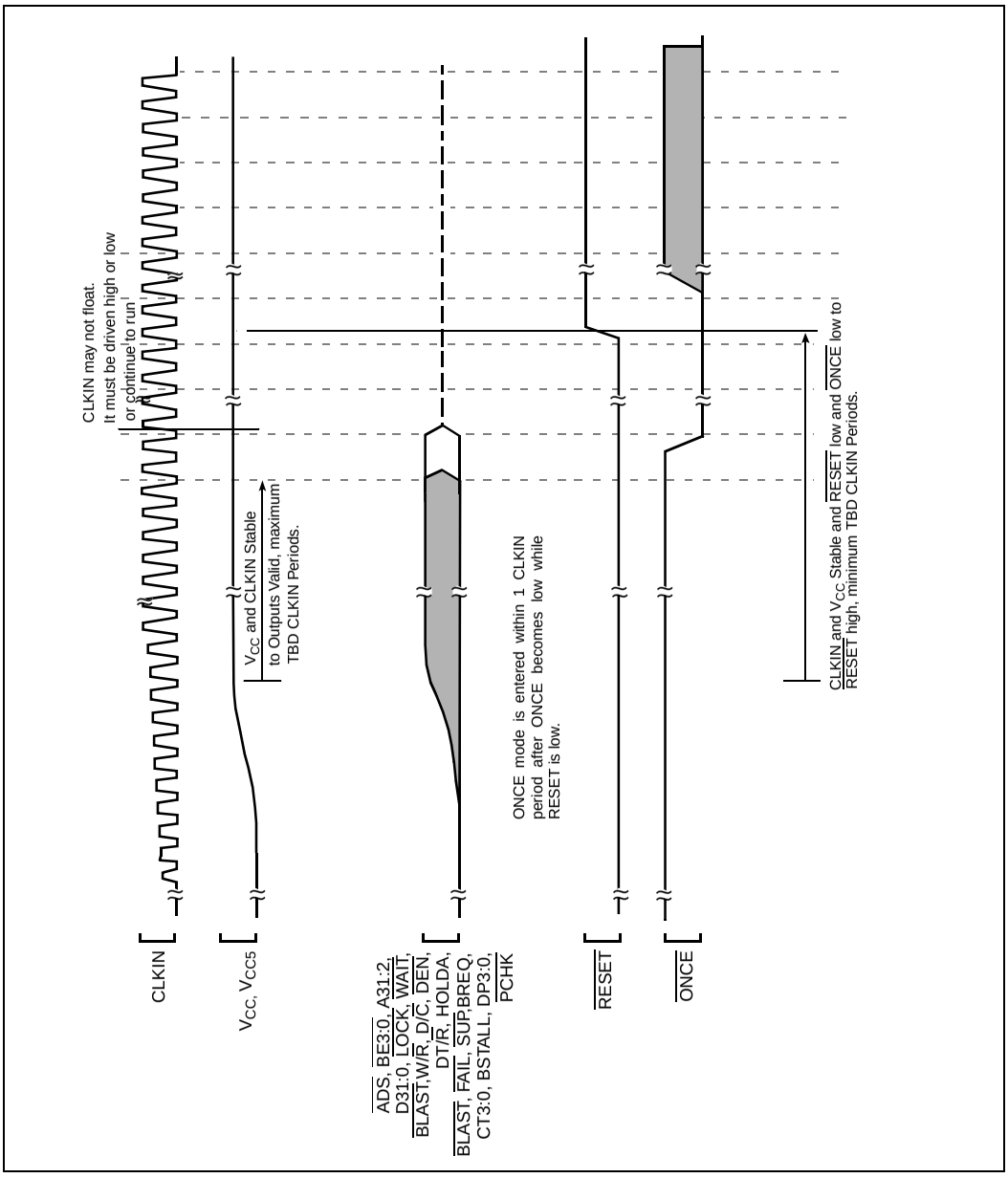


Figure 27. Entering ONCE Mode

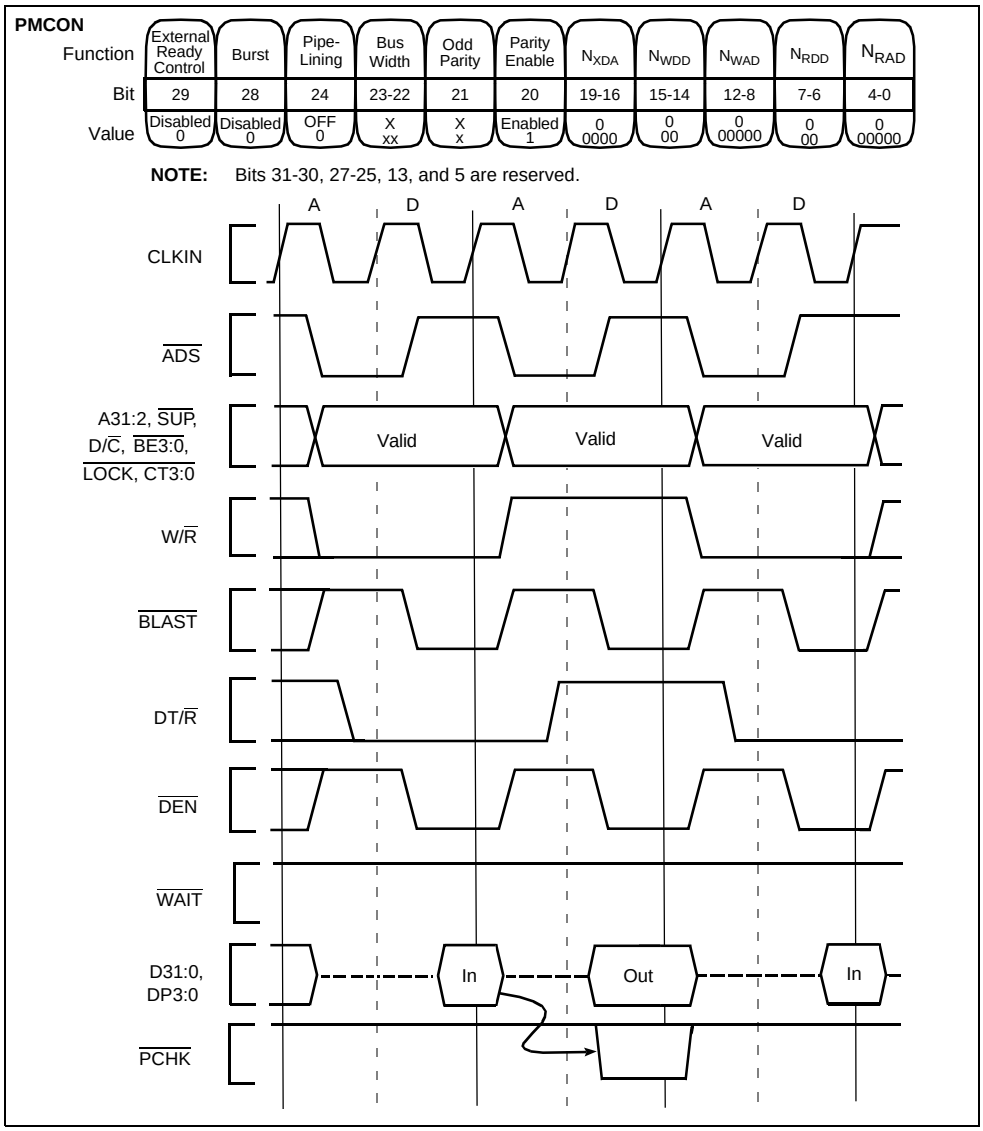


Figure 28. Non-Burst, Non-Pipelined Requests without Wait States

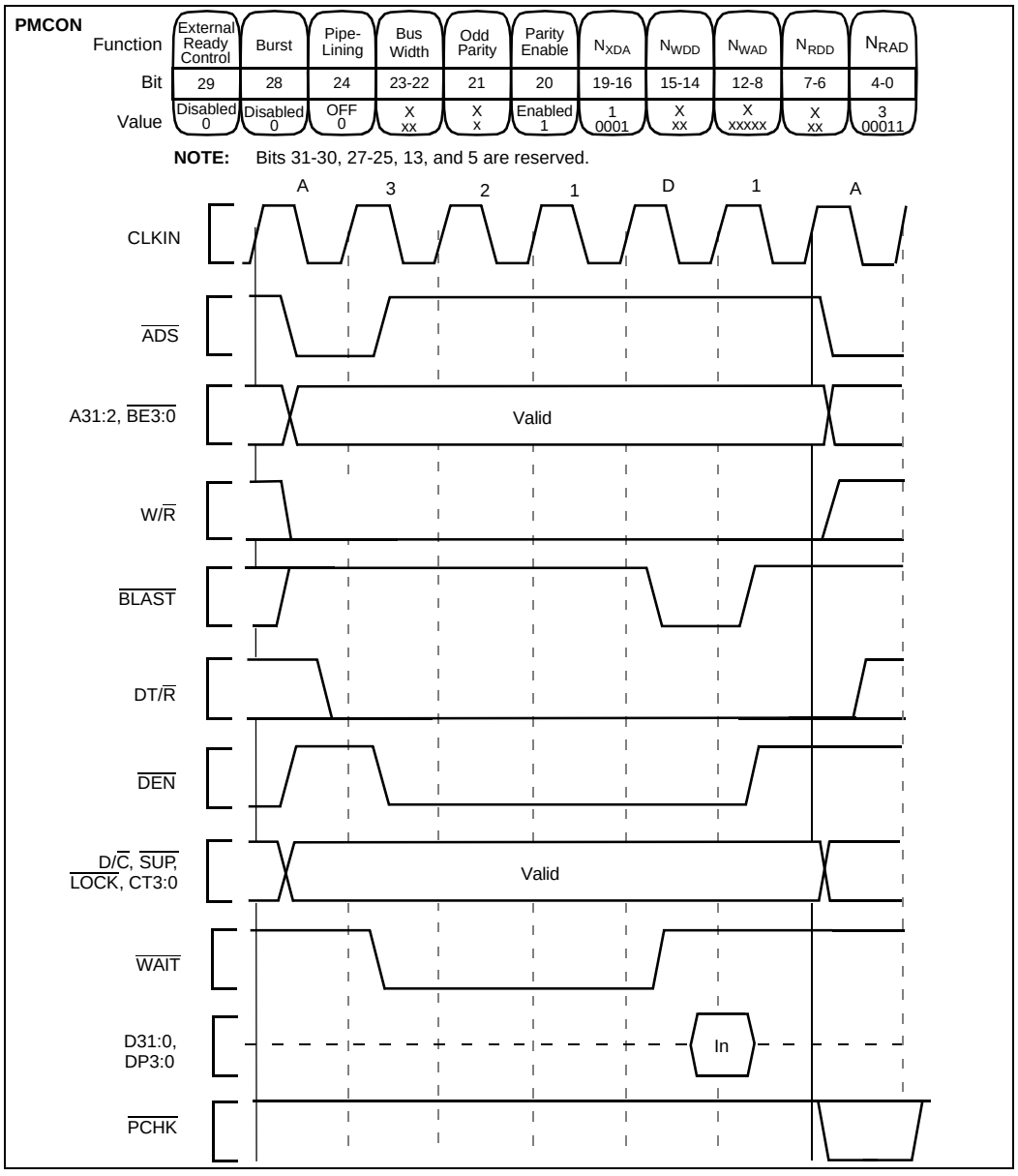


Figure 29. Non-Burst, Non-Pipelined Read Request with Wait States

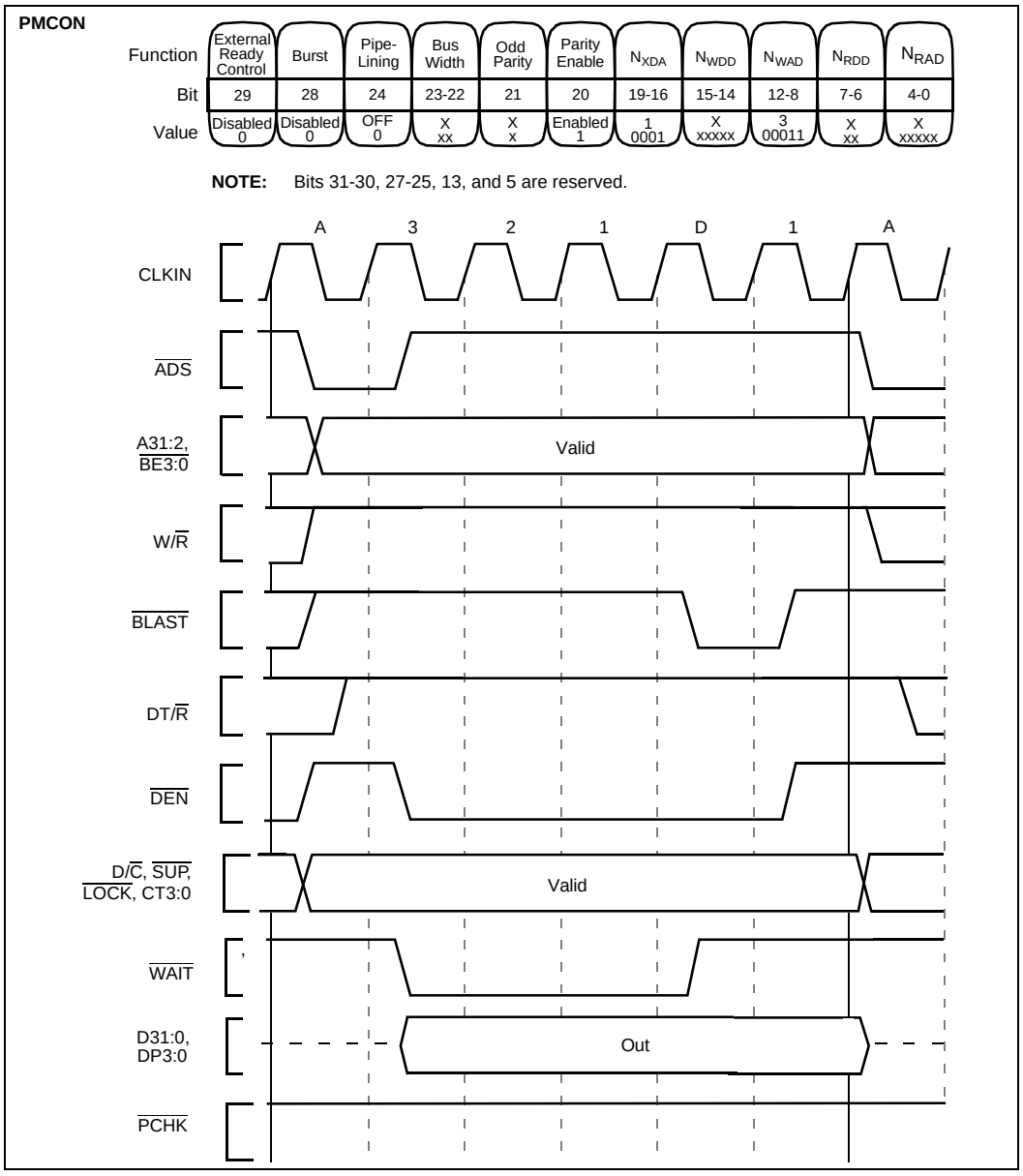


Figure 30. Non-Burst, Non-Pipelined Write Request with Wait States

PMCON

Function	External Ready Control	Burst	Pipe-Lining	Bus Width	Odd Parity	Parity Enable	N_{XDA}	N_{WDD}	N_{WAD}	N_{RDD}	N_{RAD}
Bit	29	28	24	23-22	21	20	19-16	15-14	12-8	7-6	4-0
Value	Disabled 0	Enabled 1	OFF 0	32-Bit 10	X x	Enabled 1	0 0000	X xx	X xxxxx	0 00	0 00000

NOTE: Bits 31-30, 27-25, 13, and 5 are reserved.

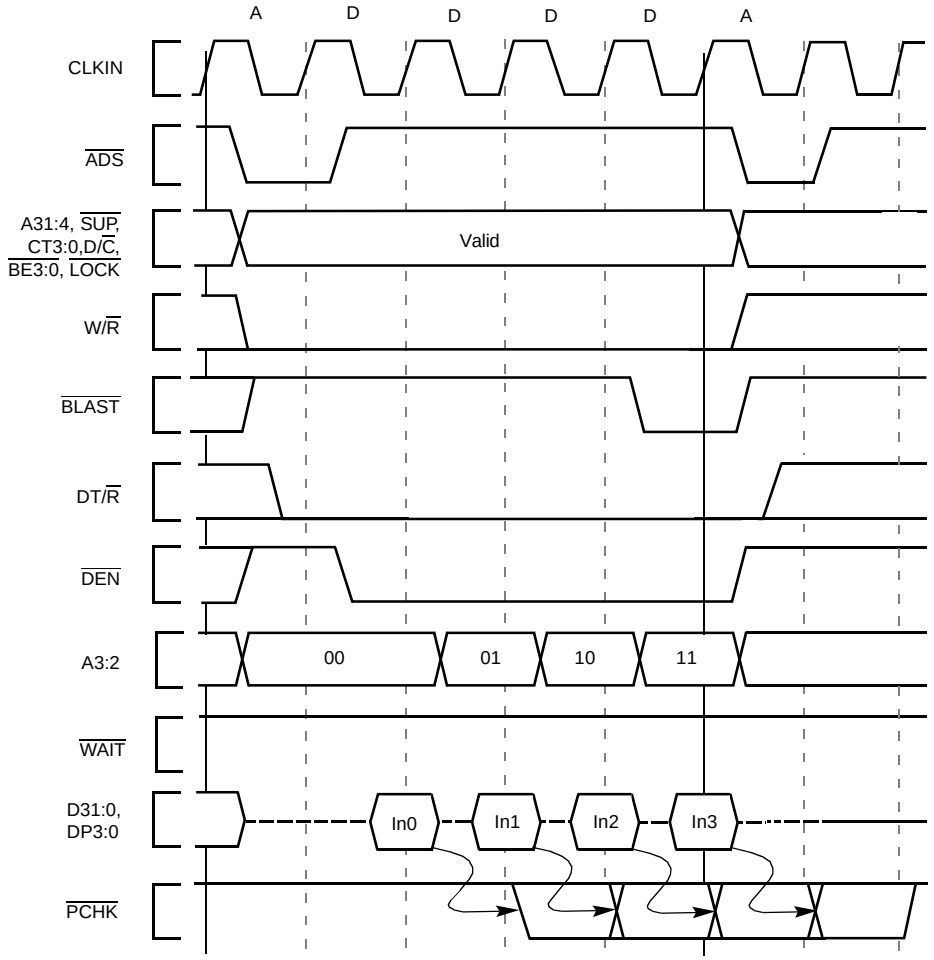


Figure 31. Burst, Non-Pipelined Read Request without Wait States, 32-Bit Bus

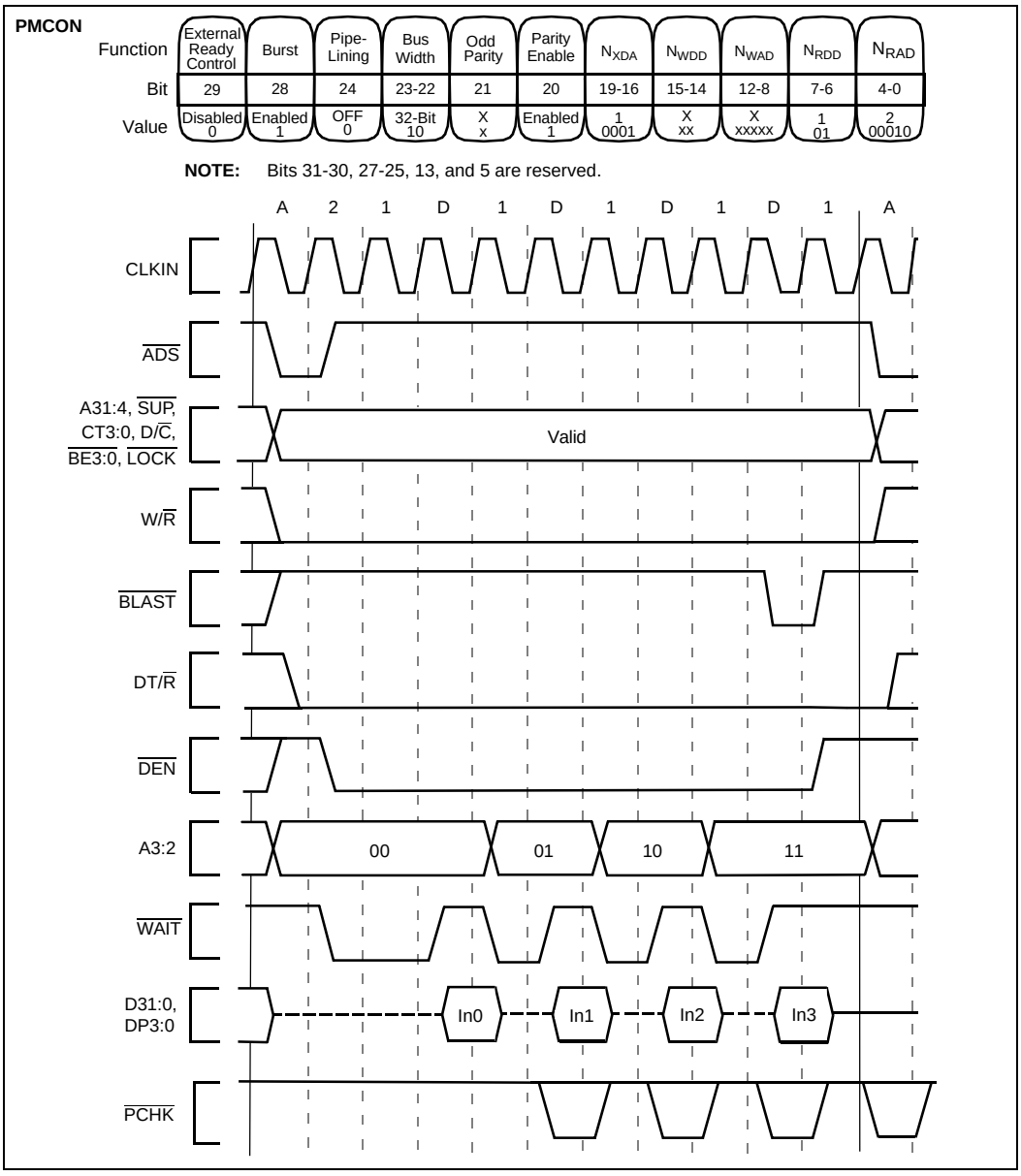


Figure 32. Burst, Non-Pipelined Read Request with Wait States, 32-Bit Bus

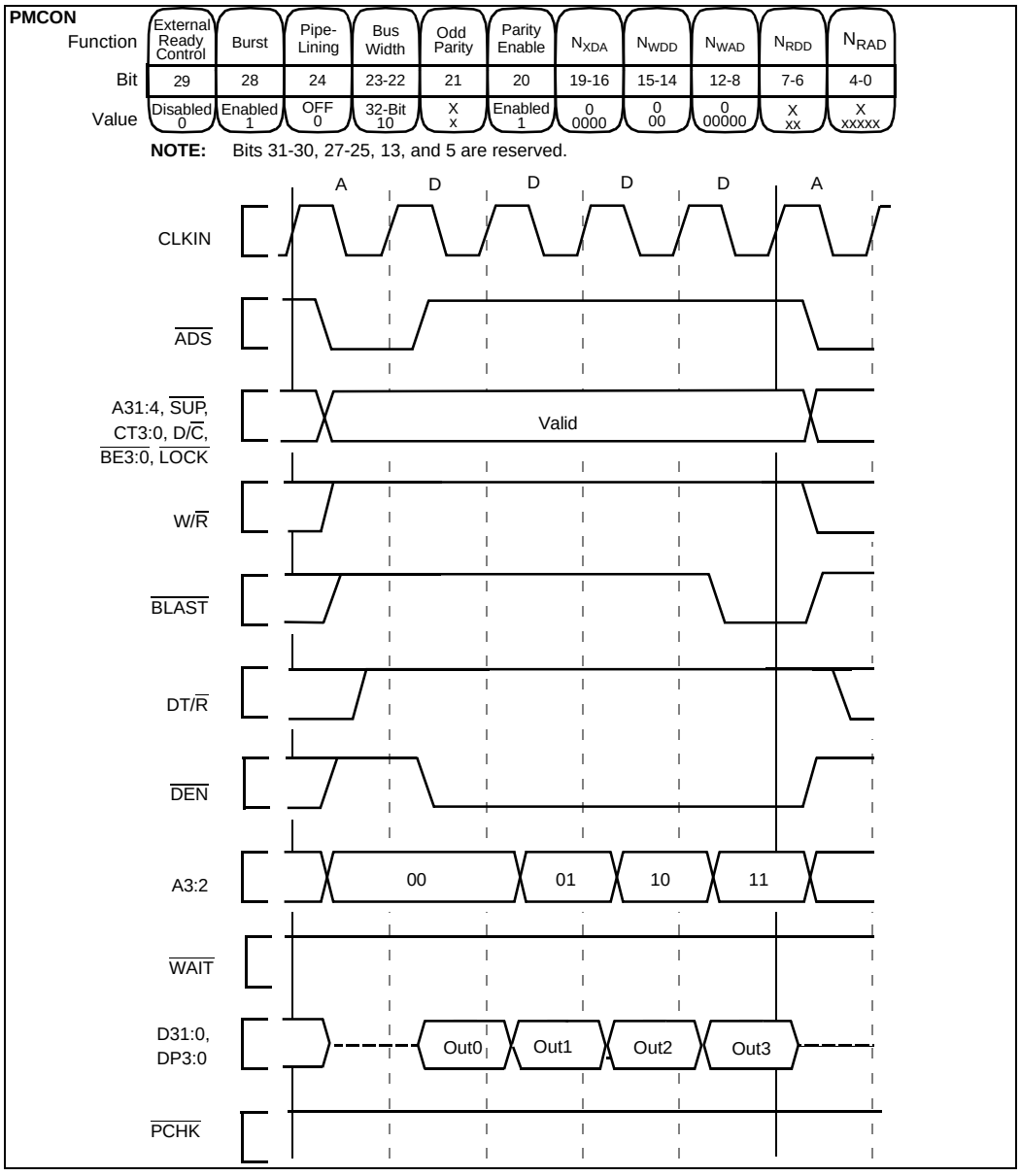


Figure 33. Burst, Non-Pipelined Write Request without Wait States, 32-Bit Bus

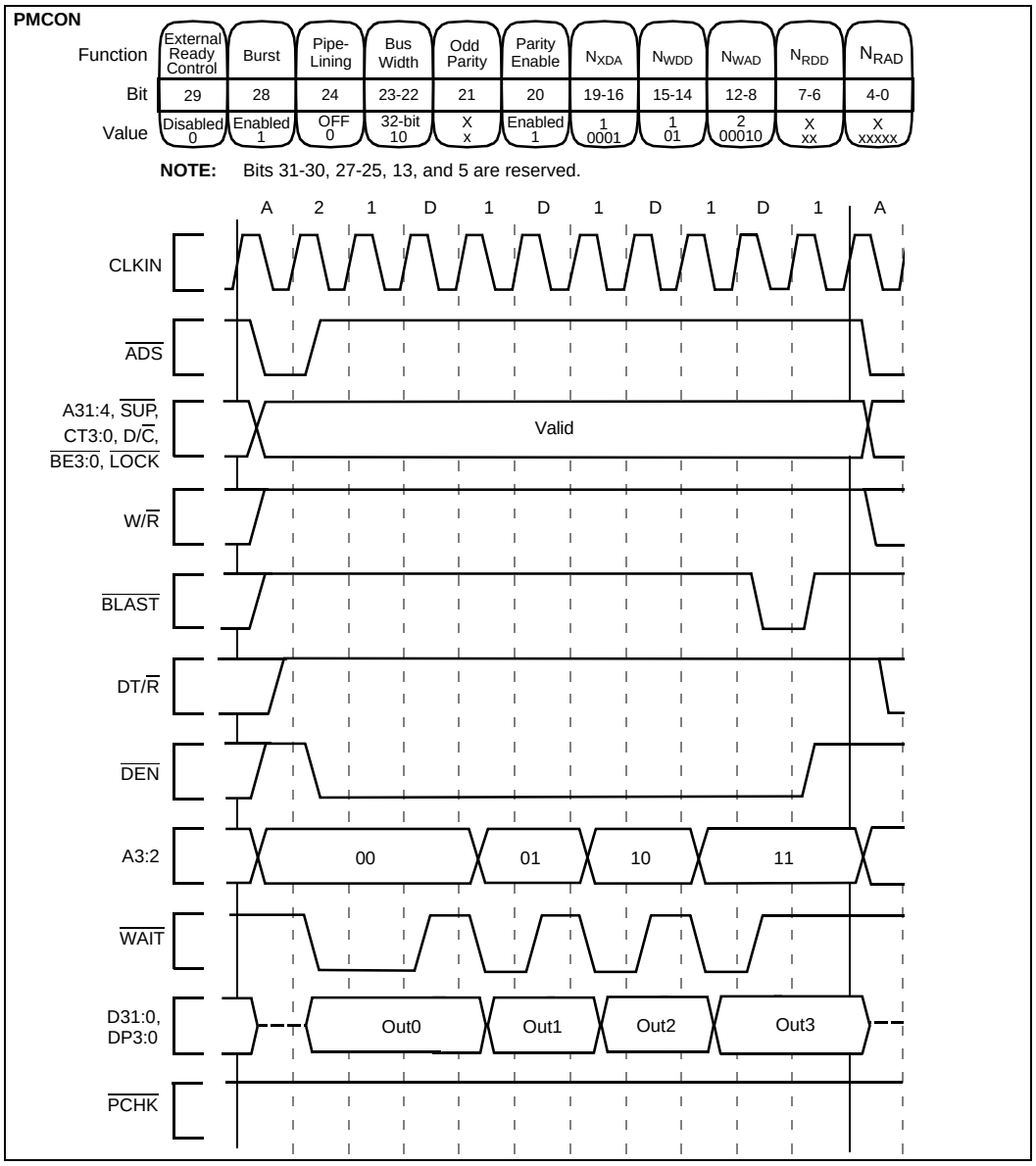


Figure 34. Burst, Non-Pipelined Write Request with Wait States, 32-Bit Bus

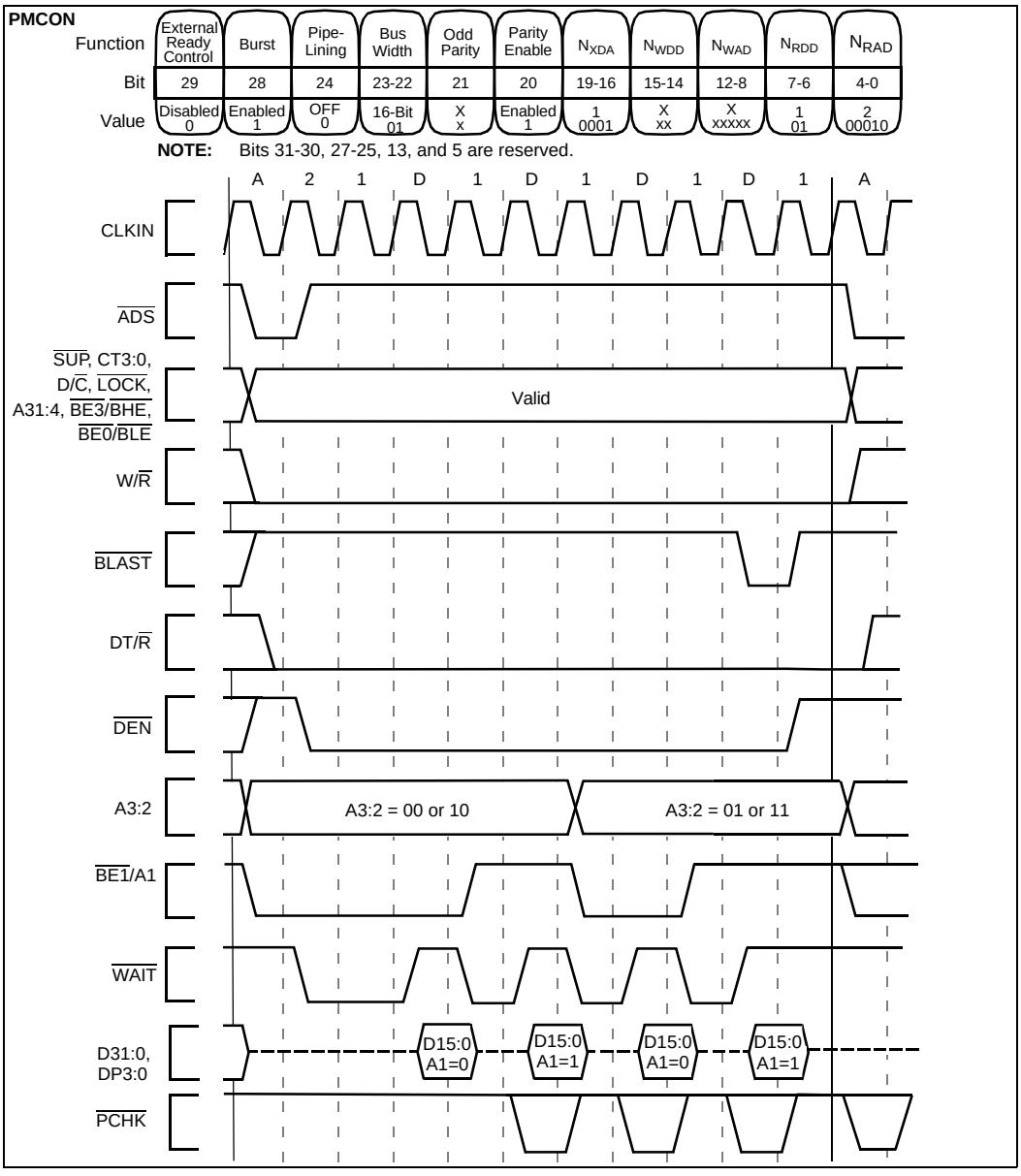


Figure 35. Burst, Non-Pipelined Read Request with Wait States, 16-Bit Bus

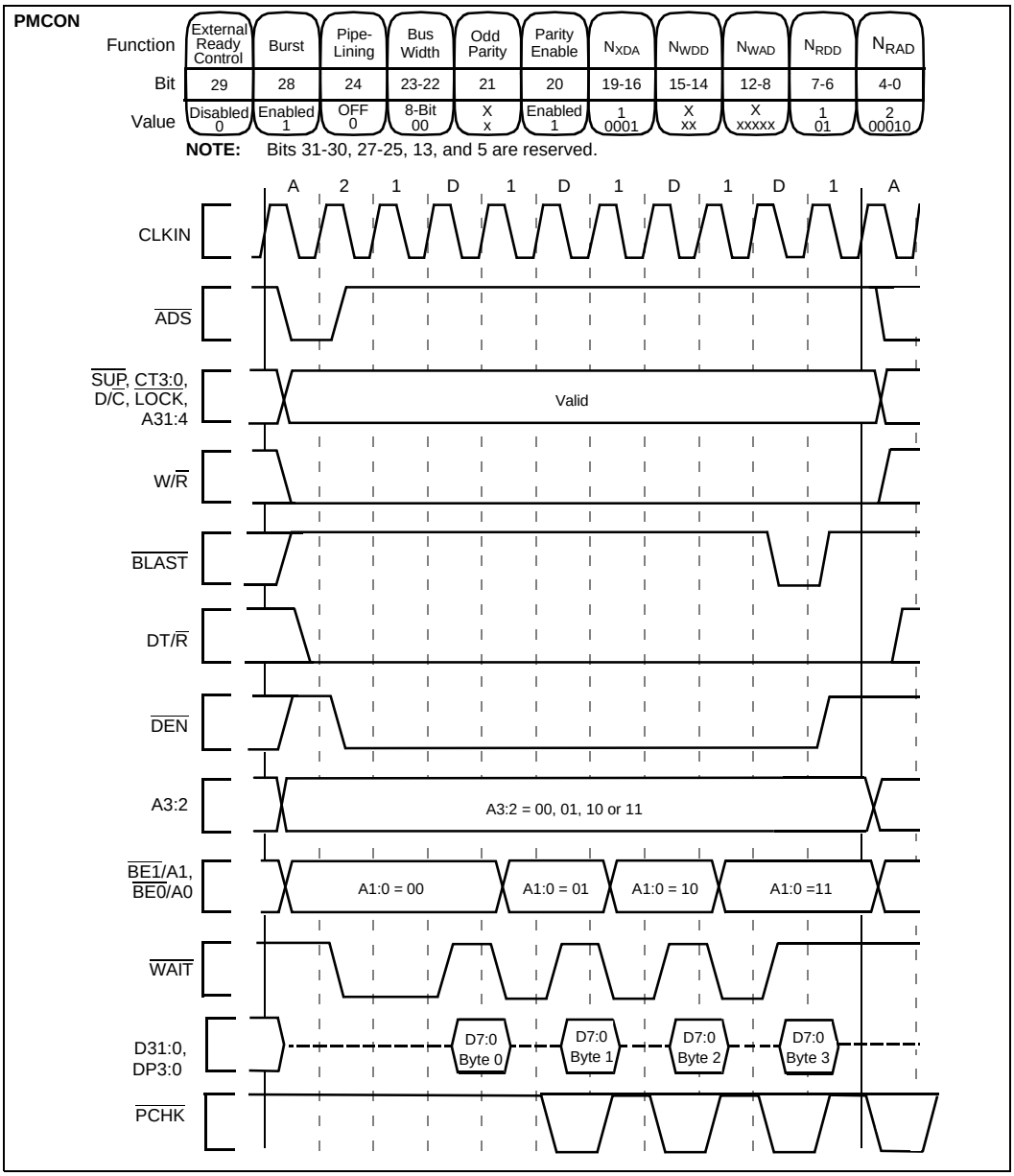


Figure 36. Burst, Non-Pipelined Read Request with Wait States, 8-Bit Bus

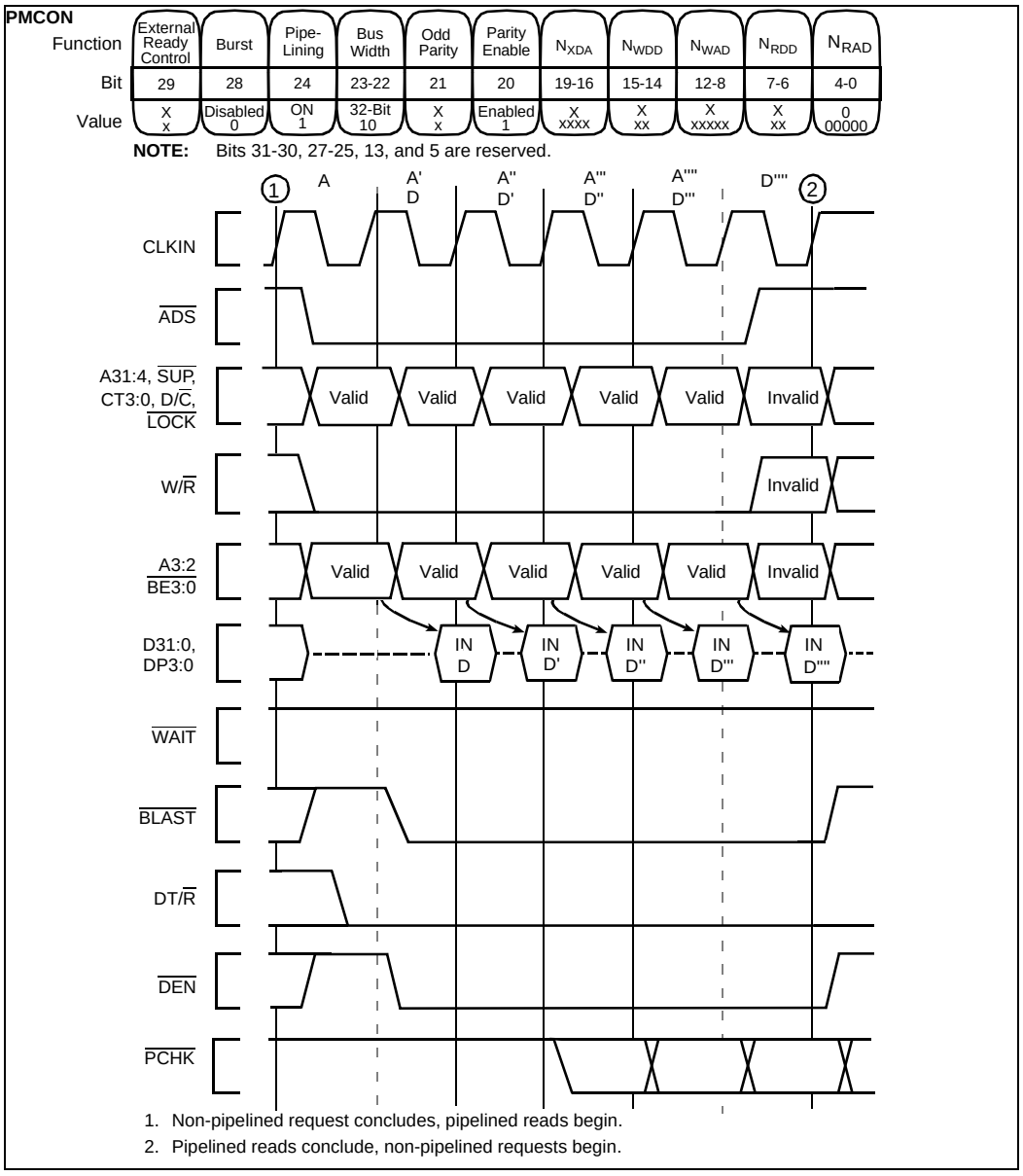


Figure 37. Non-Burst, Pipelined Read Request without Wait States, 32-Bit Bus

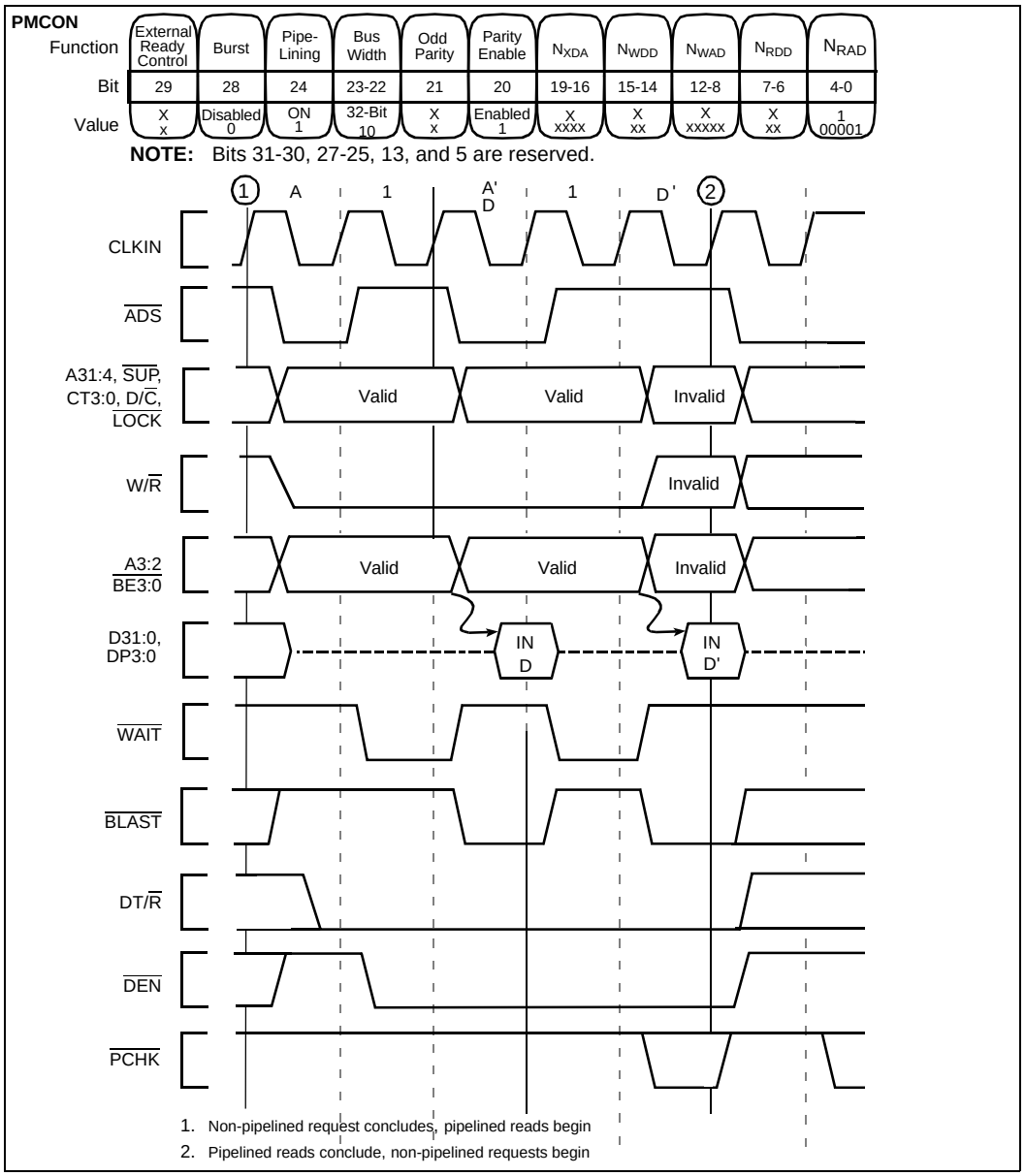


Figure 38. Non-Burst, Pipelined Read Request with Wait States, 32-Bit Bus

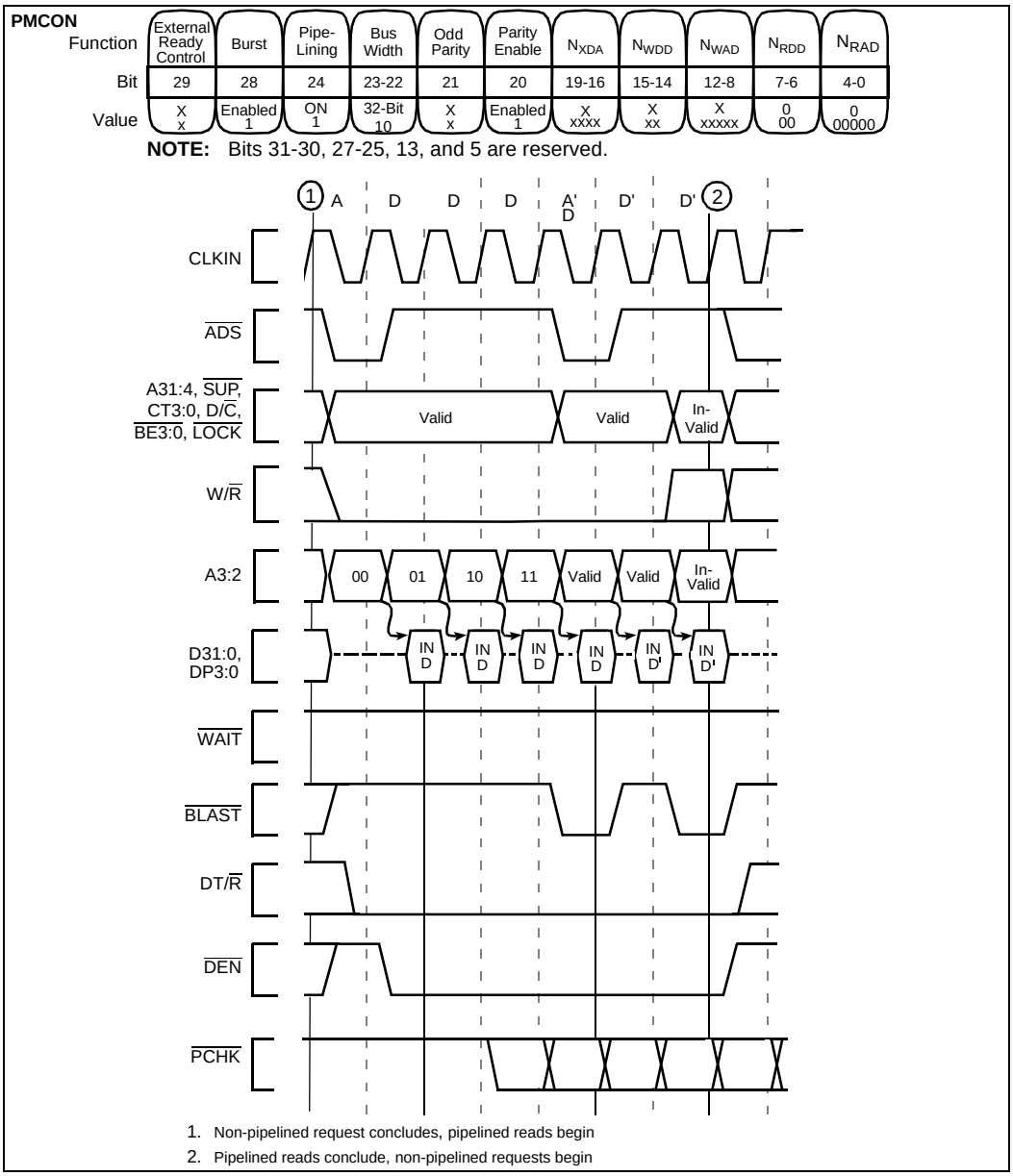
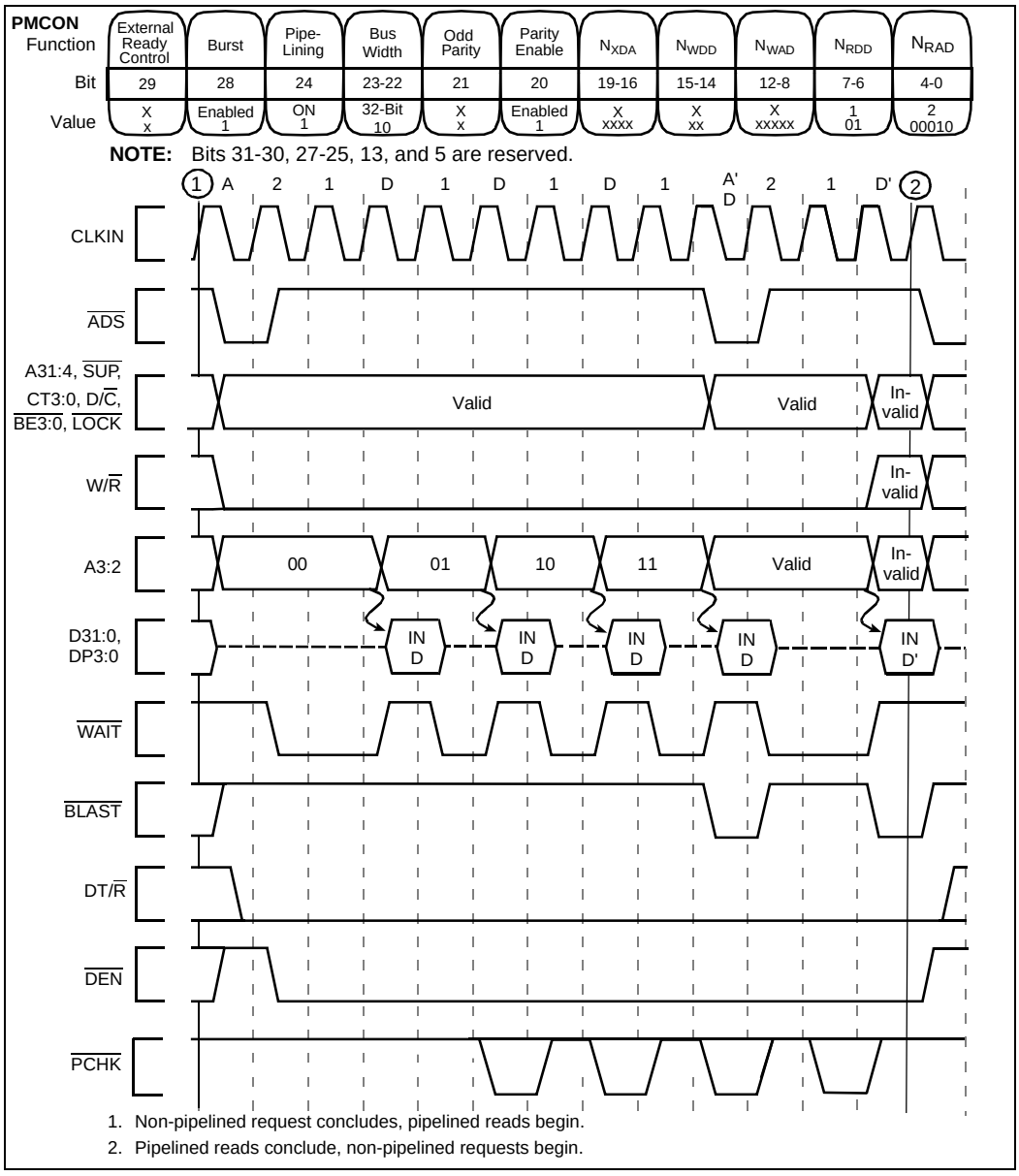


Figure 39. Burst, Pipelined Read Request without Wait States, 32-Bit Bus



1. Non-pipelined request concludes, pipelined reads begin.
2. Pipelined reads conclude, non-pipelined requests begin.

Figure 40. Burst, Pipelined Read Request with Wait States, 32-Bit Bus

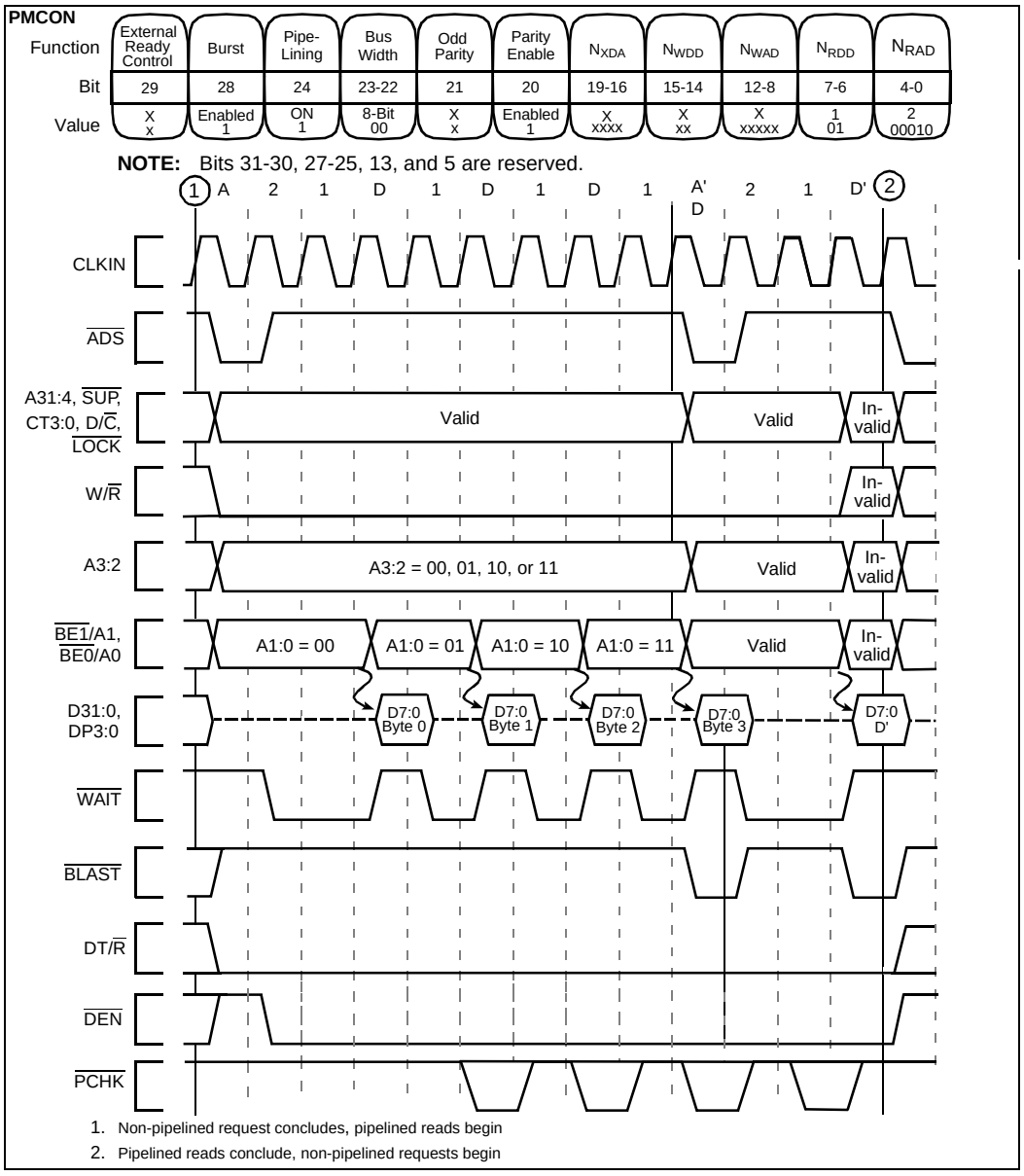


Figure 41. Burst, Pipelined Read Request with Wait States, 8-Bit Bus

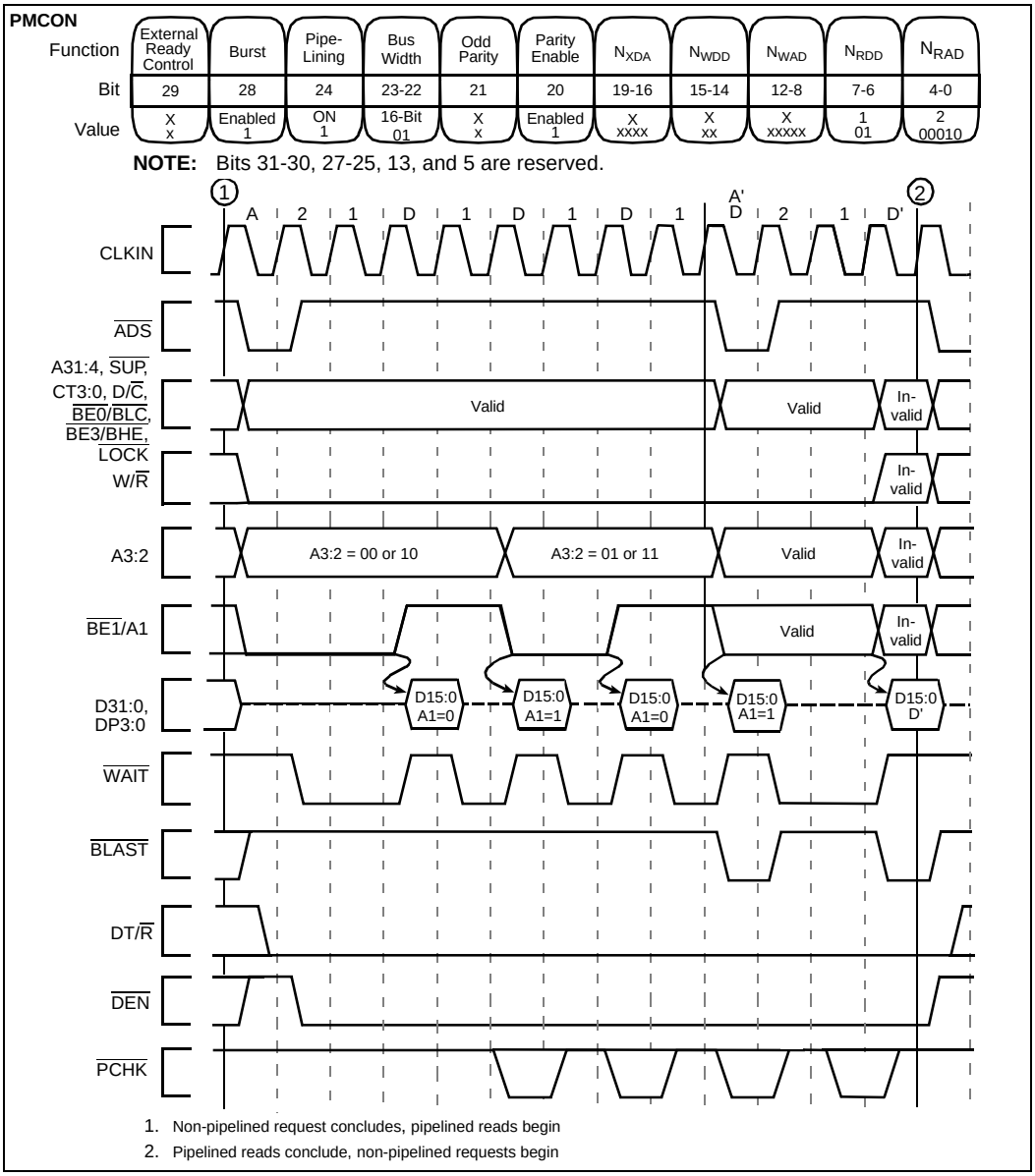
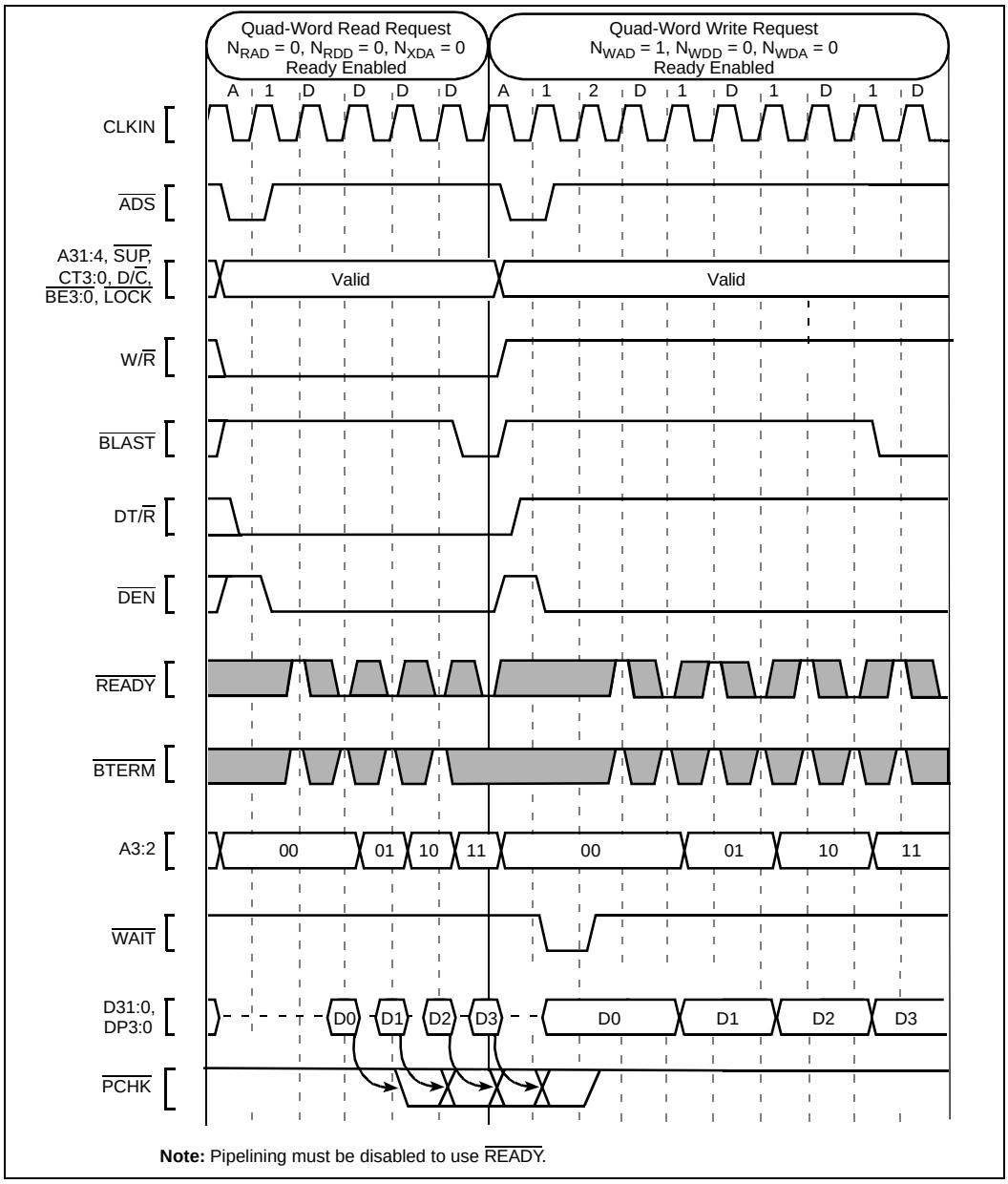
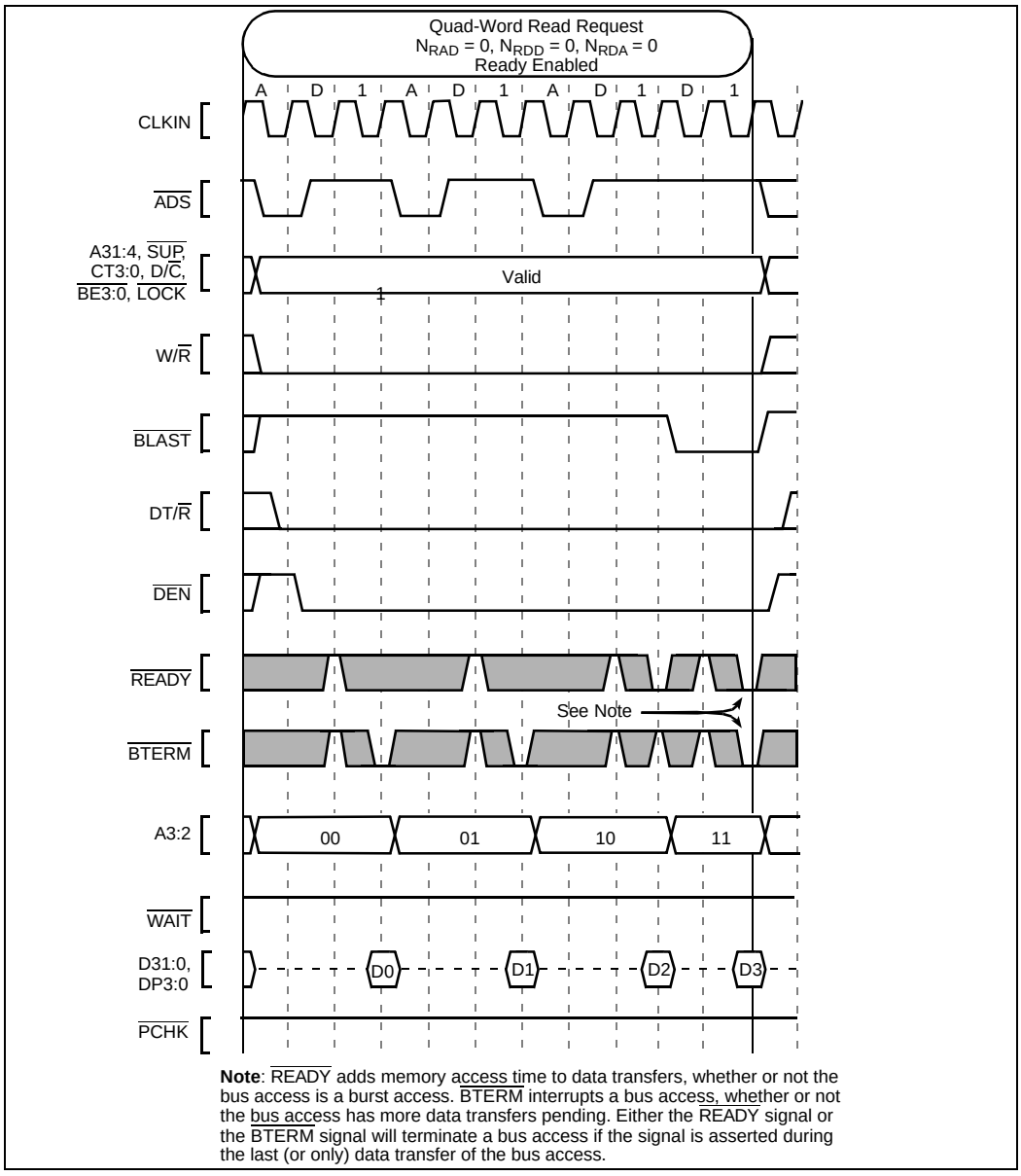


Figure 42. Burst, Pipelined Read Request with Wait States, 16-Bit Bus



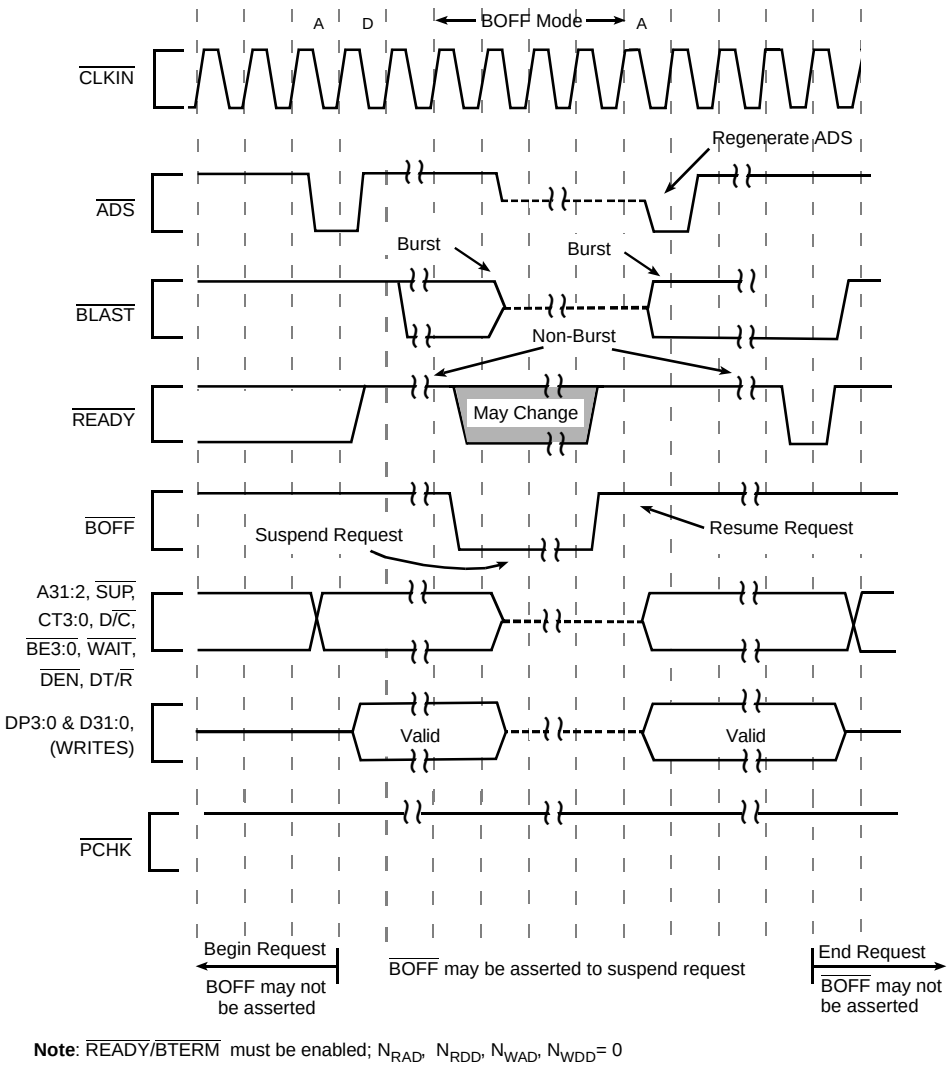
Note: Pipelining must be disabled to use READY.

Figure 43. Using External READY



Note: READY adds memory access time to data transfers, whether or not the bus access is a burst access. BTERM interrupts a bus access, whether or not the bus access has more data transfers pending. Either the READY signal or the BTERM signal will terminate a bus access if the signal is asserted during the last (or only) data transfer of the bus access.

Figure 44. Terminating a Burst with BTERM



Note: READY/BTERM must be enabled; N_{RAD}, N_{RDD}, N_{WAD}, N_{WDD}= 0

Figure 45. BOFF Functional Timing

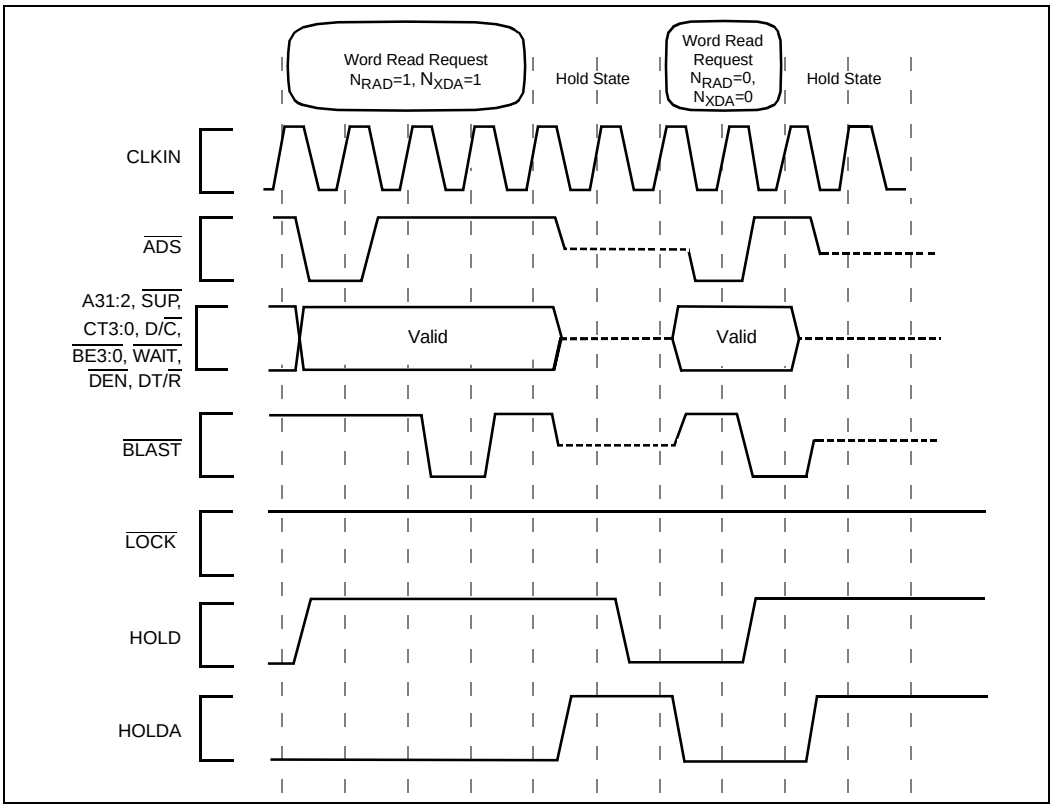


Figure 46. HOLD Functional Timing

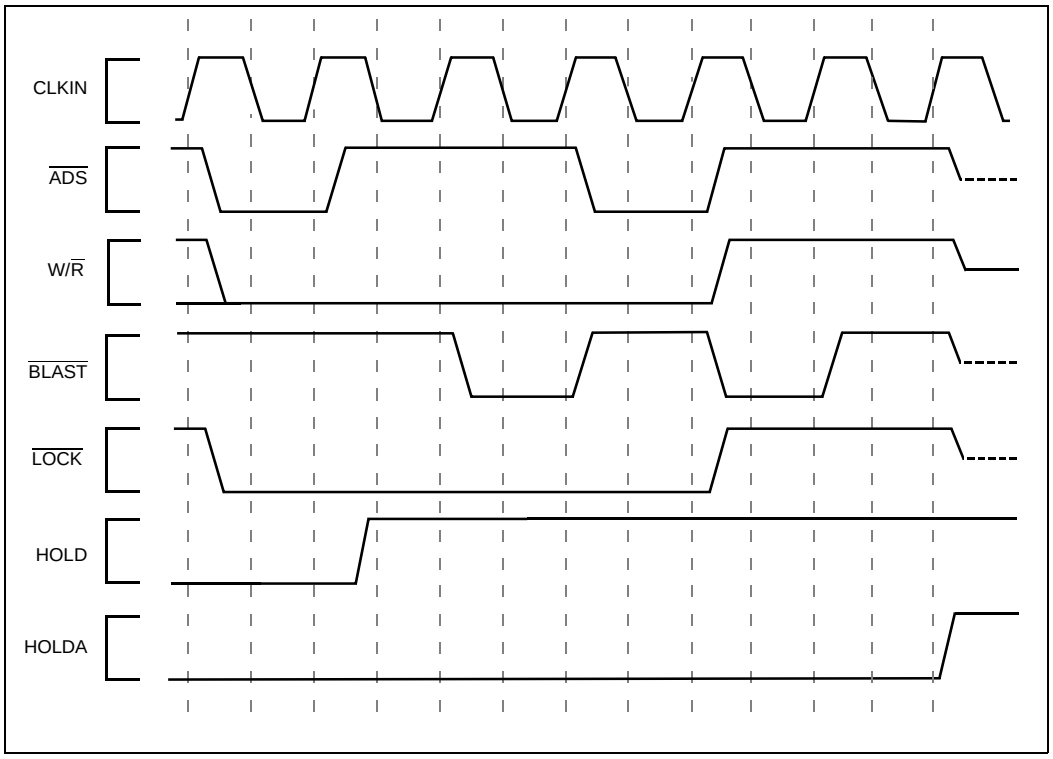


Figure 47. Lock Delays HOLDA Timing

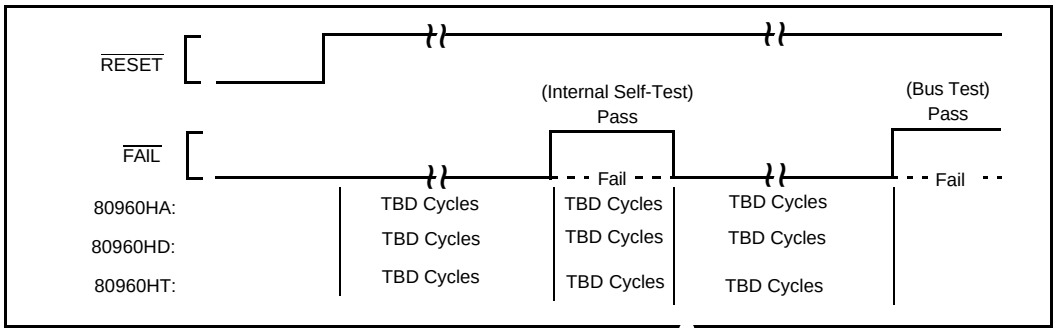
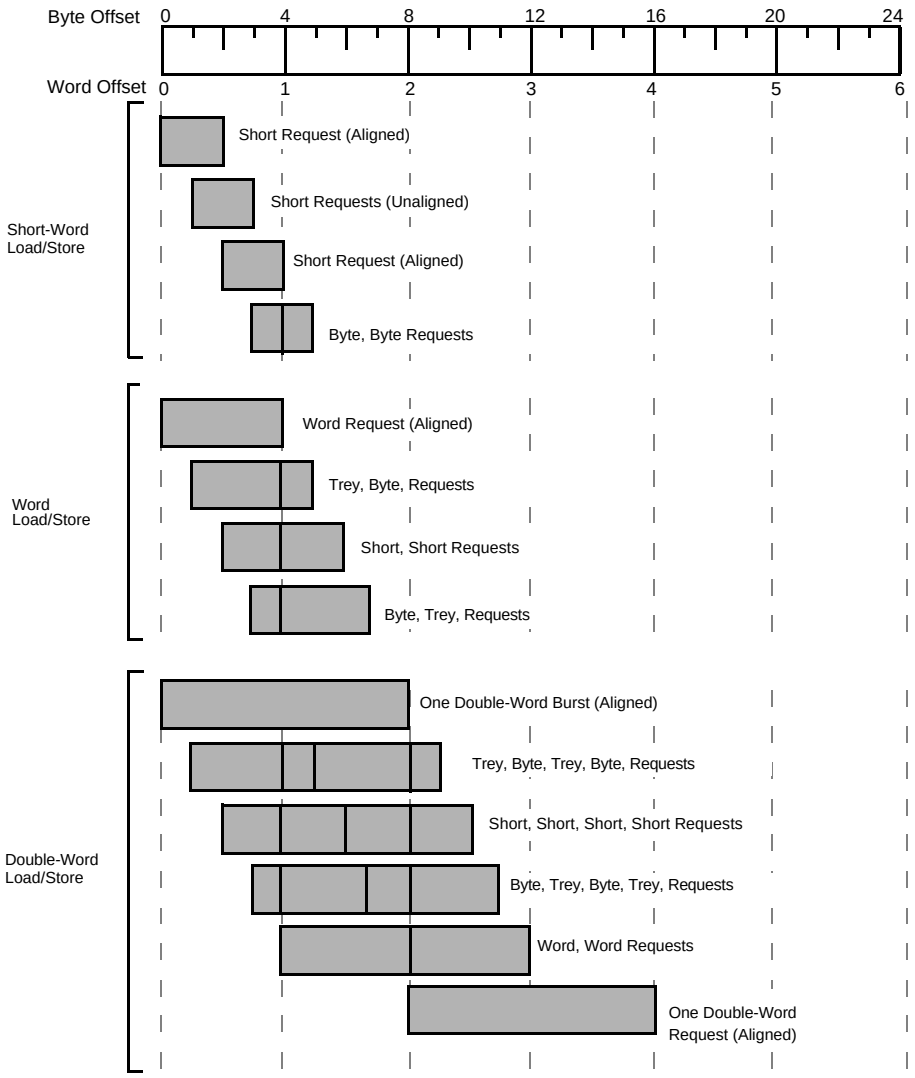


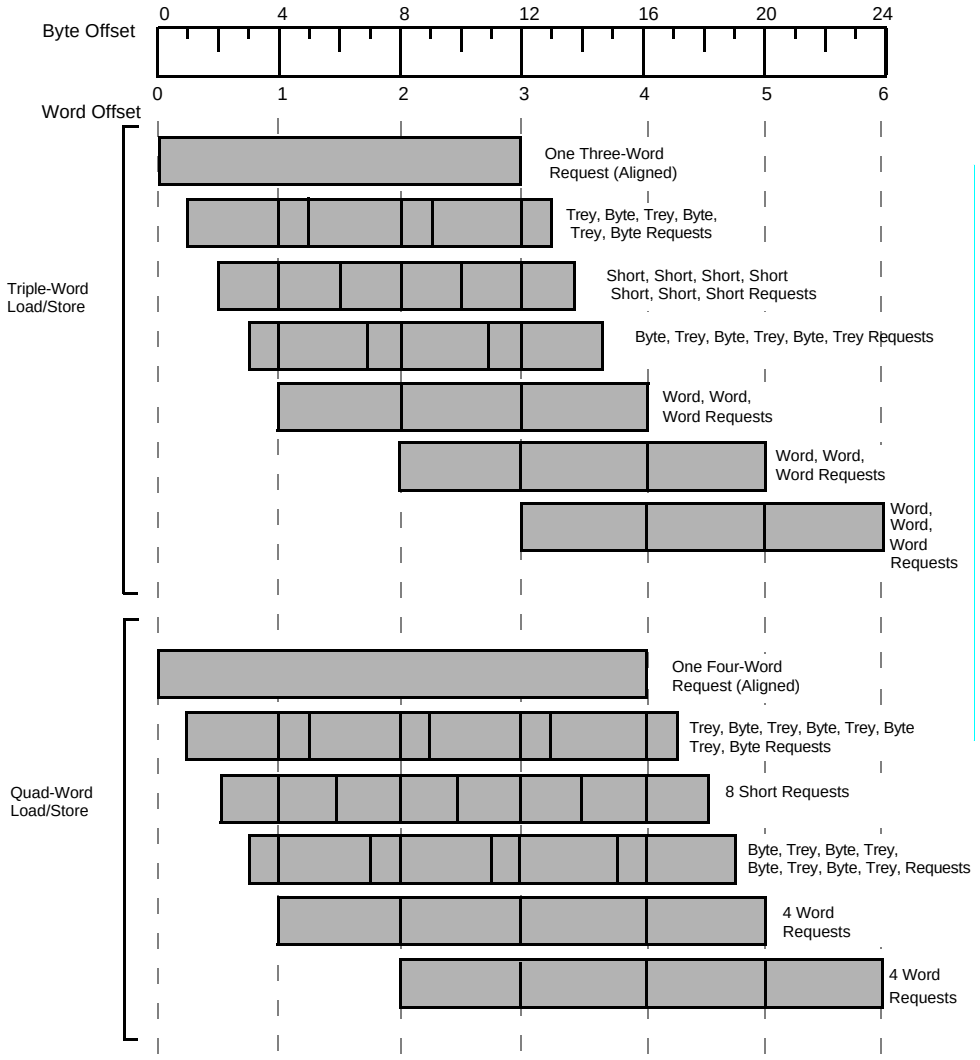
Figure 48. FAIL Functional Timing



NOTES:

1. All requests which are less than a word in size and are cacheable will be promoted to a word to be cached. This causes adjacent requests to occur for full words to the same address.

Figure 49. A Summary of Aligned and Unaligned Transfers for 32-Bit Regions



NOTES:

1. All requests which are less than a word in size and are cacheable will be promoted to a word to be cached. This causes adjacent requests to occur for full words to the same address.

Figure 50. A Summary of Aligned and Unaligned Transfers for 32-Bit Regions (Continued)

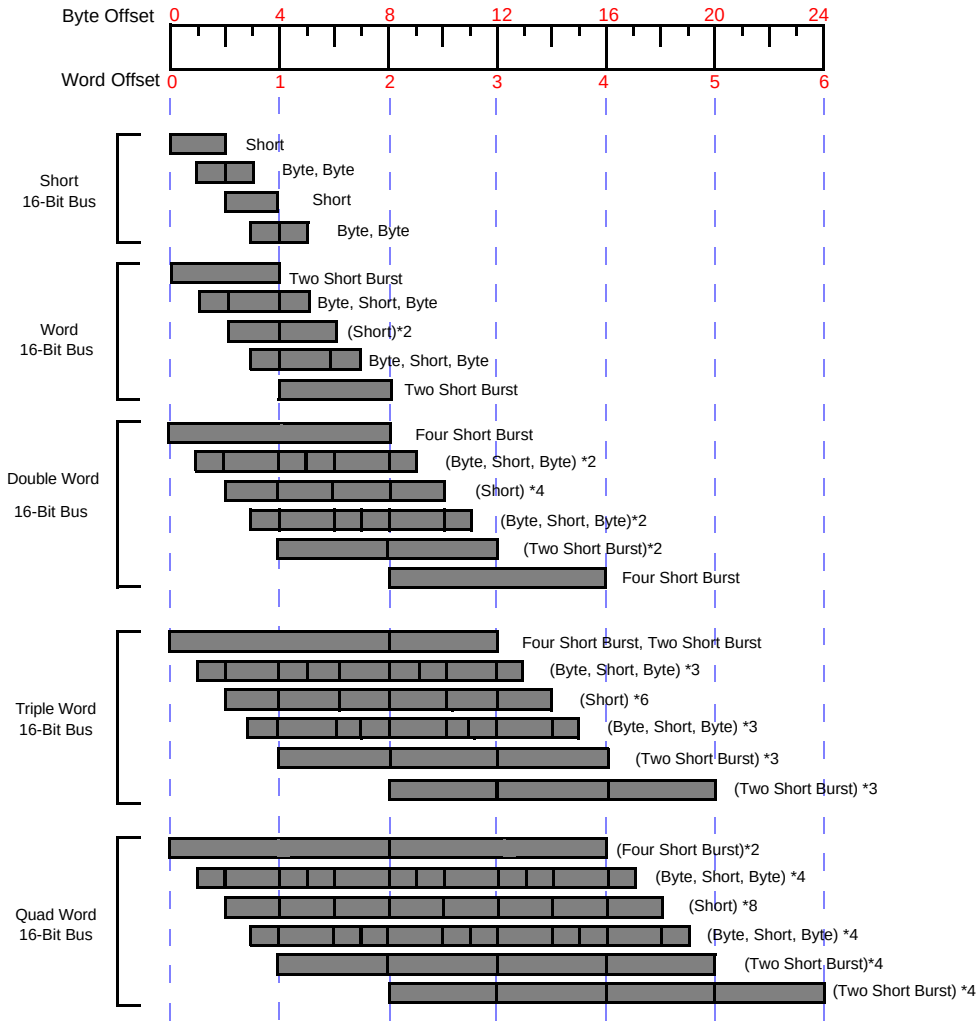


Figure 51. A Summary of Aligned and Unaligned Transfers for 16-Bit Bus

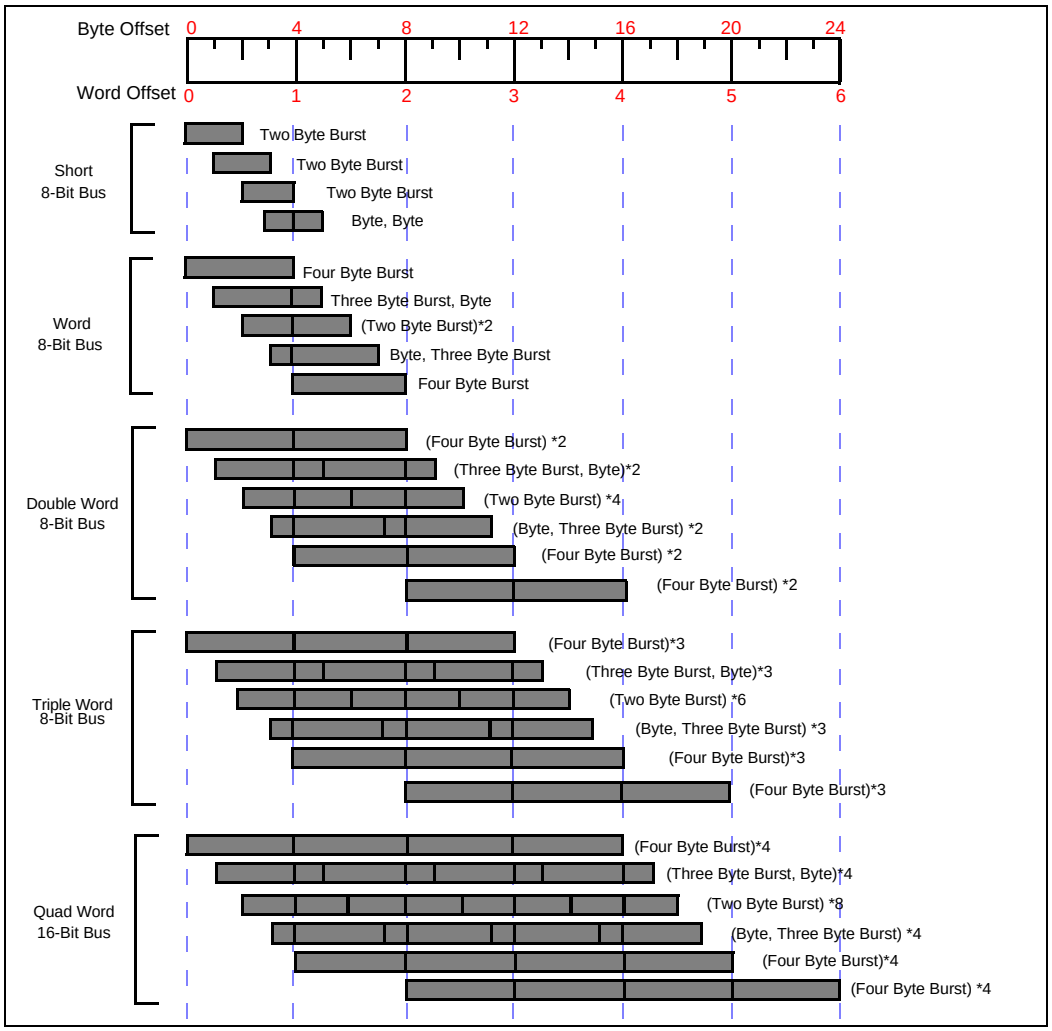


Figure 52. A Summary of Aligned and Unaligned Transfers for 8-Bit Bus

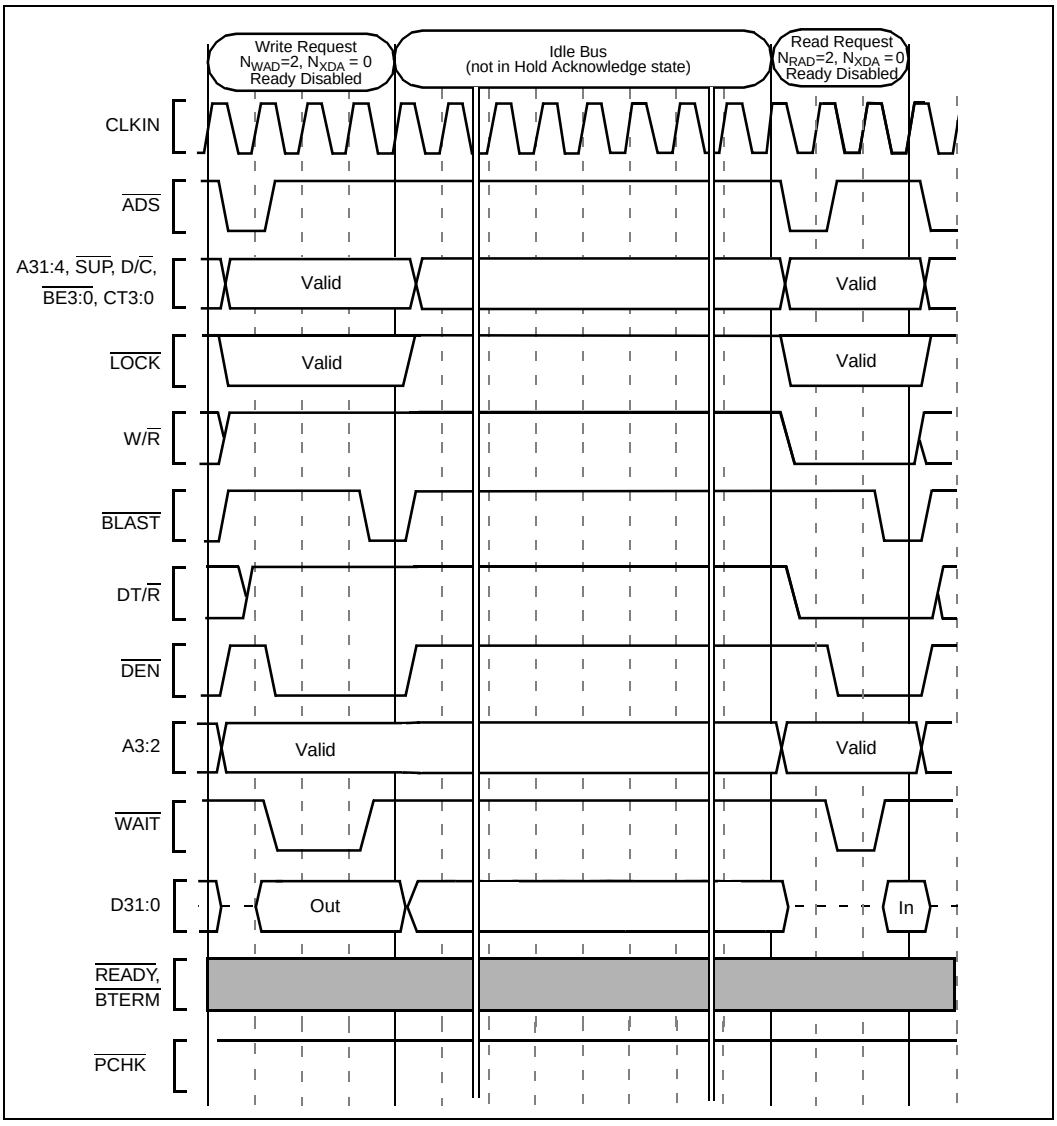
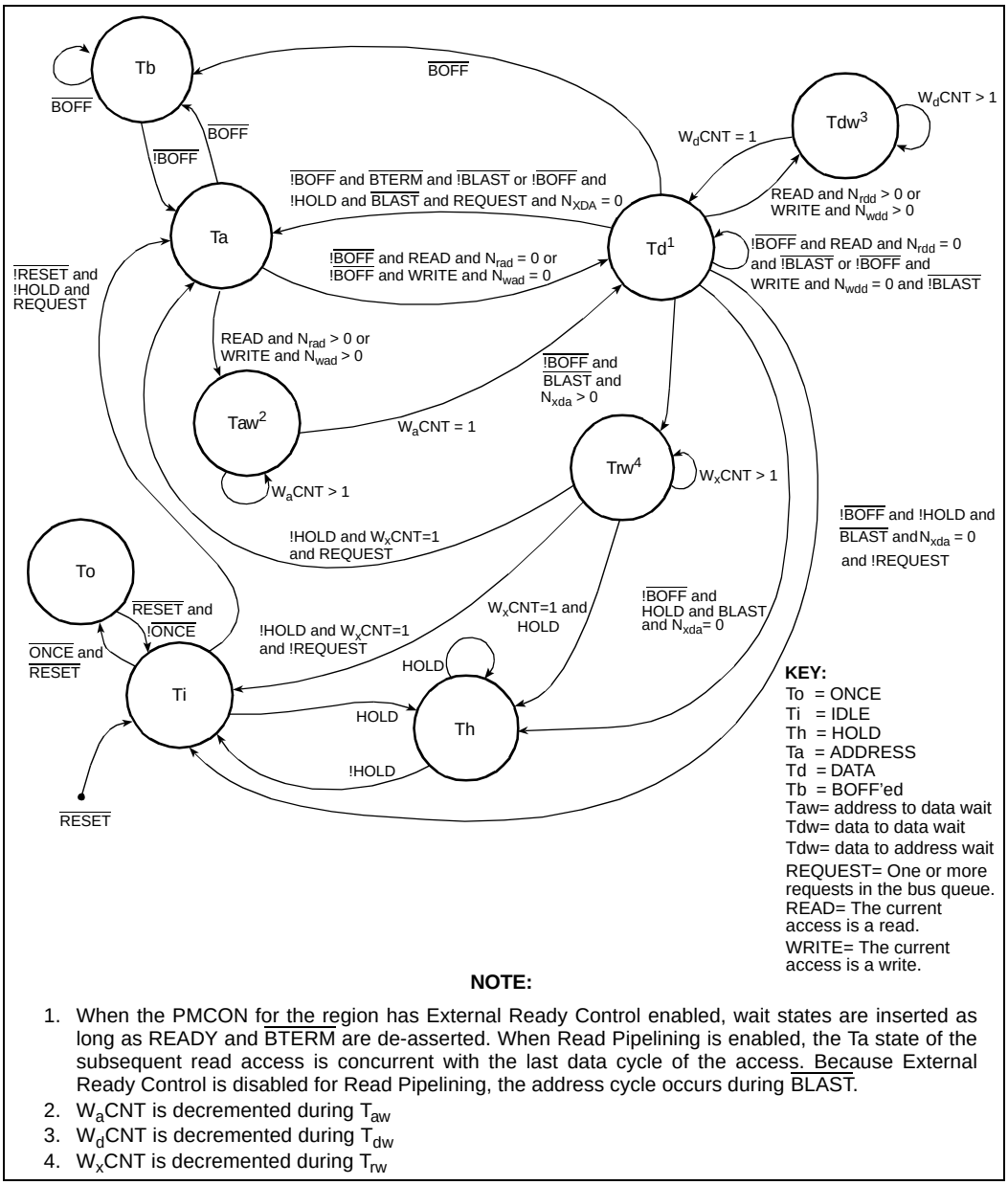


Figure 53. Idle Bus Operation



NOTE:

1. When the PMCON for the region has External Ready Control enabled, wait states are inserted as long as READY and BTERM are de-asserted. When Read Pipelining is enabled, the Ta state of the subsequent read access is concurrent with the last data cycle of the access. Because External Ready Control is disabled for Read Pipelining, the address cycle occurs during BLAST.
2. W_aCNT is decremented during T_{aw}
3. W_dCNT is decremented during T_{dw}
4. W_xCNT is decremented during T_{rw}

Figure 54. Bus States

5.1 80960Hx Boundary Scan Chain

Table 23. 80960Hx Boundary Scan Chain (Sheet 1 of 5)

#	BOUNDARY SCAN CELL	CELL TYPE	COMMENT
1	DP3	Bidirectional	
2	DP2	Bidirectional	
3	DP0	Bidirectional	
4	DP1	Bidirectional	
5	STEST	Input	
6	FAILBAR	Output	
7	Enable for FAILBAR, BSTALL and BREQ	Control	
8	ONCEBAR	Input	
9	BOFFBAR	Input	
10	D0	Bidirectional	
11	D1	Bidirectional	
12	D2	Bidirectional	
13	D3	Bidirectional	
14	D4	Bidirectional	
15	D5	Bidirectional	
16	D6	Bidirectional	
17	D7	Bidirectional	
18	Enable for DP(3:0) and D(31:0)	Control	
19	D8	Bidirectional	
20	D9	Bidirectional	
21	D10	Bidirectional	
22	D11	Bidirectional	
23	D12	Bidirectional	
24	D13	Bidirectional	
25	D14	Bidirectional	
26	D15	Bidirectional	
27	D16	Bidirectional	

NOTES:
1. Cell#1 connects to TDO and cell #112 connects to TDI.
2. All outputs are three-state.
3. In output and bidirectional signals, a logical 1 on the enable signal enables the output. A logical 0 three-states the output.

Table 23. 80960Hx Boundary Scan Chain (Sheet 2 of 5)

#	BOUNDARY SCAN CELL	CELL TYPE	COMMENT
28	D17	Bidirectional	
29	D18	Bidirectional	
30	D19	Bidirectional	
31	D20	Bidirectional	
32	D21	Bidirectional	
33	D22	Bidirectional	
34	D23	Bidirectional	
35	D24	Bidirectional	
36	D25	Bidirectional	
37	D26	Bidirectional	
38	D27	Bidirectional	
39	D28	Bidirectional	
40	D29	Bidirectional	
41	D30	Bidirectional	
42	D31	Bidirectional	
43	BTERMBAR	Input	
44	RDYBAR	Input	Appears as READYBAR in BSDL file.
45	HOLD	Input	
46	HOLDA	Output	
47	Enable for HOLDA control	Control	
48	ADSBAR	Output	
49	BE3BAR	Output	Appears as BEBAR(3) in BSDL file.
50	BE2BAR	Output	
51	BE1BAR	Output	
52	BE0BAR	Output	
53	BLASTBAR	Output	
54	DENBAR	Output	
55	WRRDBAR	Output	Appears as WRBAR in BSDL file.

NOTES:

1. Cell#1 connects to TDO and cell #112 connects to TDI.
2. All outputs are three-state.
3. In output and bidirectional signals, a logical 1 on the enable signal enables the output. A logical 0 three-states the output.

Table 23. 80960Hx Boundary Scan Chain (Sheet 3 of 5)

#	BOUNDARY SCAN CELL	CELL TYPE	COMMENT
56	DTRBAR	Output	
57	Enable for DTRBAR	Control	
58	WAITBAR	Output	
59	BSTALL	Output	
60	DATACODBAR	Output	Appears as DCBAR in BSDL file.
61	USERSUPBAR	Output	Appears as SUPBAR in BSDL file.
62	Enable for ADSBAR, BEBAR, BLASTBAR, DENBAR, WRRDBAR, WAITBAR, DCBAR, SUPBAR and LOCKBAR,	Control	
63	LOCKBAR	Output	
64	BREQ	Output	
65	A31	Output	
66	A30	Output	
67	A29	Output	
68	A28	Output	
69	A27	Output	
70	A26	Output	
71	A25	Output	
72	A24	Output	
73	A23	Output	
74	A22	Output	
75	A21	Output	
76	A20	Output	
77	A19	Output	
78	A18	Output	
79	A17	Output	
80	A16	Output	
81	Enable for A(31:0) and CT(3:)	Control	
82	A15	Output	

NOTES:

1. Cell#1 connects to TDO and cell #112 connects to TDI.
2. All outputs are three-state.
3. In output and bidirectional signals, a logical 1 on the enable signal enables the output. A logical 0 three-states the output.

Table 23. 80960Hx Boundary Scan Chain (Sheet 4 of 5)

#	BOUNDARY SCAN CELL	CELL TYPE	COMMENT
83	A14	Output	
84	A13	Output	
85	A12	Output	
86	A11	Output	
87	A10	Output	
88	A9	Output	
89	A8	Output	
90	A7	Output	
91	A6	Output	
92	A5	Output	
93	A4	Output	
94	A3	Output	
95	A2	Output	
96	NMIBAR	Input	
97	XINT7BAR	Input	Appears as XINTBAR(7) in BSDL file.
98	XINT6BAR	Input	
99	XINT5BAR	Input	
100	XINT4BAR	Input	
101	XINT3BAR	Input	
102	XINT2BAR	Input	
103	XINT1BAR	Input	
104	XINT0BAR	Input	
105	RESETBAR	Input	
106	CLKIN	Input	
107	CT3	Output	Appears as CT(3) in BSDL file.

NOTES:

1. Cell#1 connects to TDO and cell #112 connects to TDI.
2. All outputs are three-state.
3. In output and bidirectional signals, a logical 1 on the enable signal enables the output. A logical 0 three-states the output.

Table 23. 80960Hx Boundary Scan Chain (Sheet 5 of 5)

#	BOUNDARY SCAN CELL	CELL TYPE	COMMENT
108	CT2	Output	
109	CT1	Output	
110	CT0	Output	
111	PCHK	Output	Appears as PCHKBAR in BSDL file.
112	PCHK enable	Control	

NOTES:
1. Cell#1 connects to TDO and cell #112 connects to TDI.
2. All outputs are three-state.
3. In output and bidirectional signals, a logical 1 on the enable signal enables the output. A logical 0 three-states the output.

5.2 Boundary Scan Description Language Example

Boundary-Scan Description Language (BSDL) example 14-2 meets the de facto standard means of describing essential features of ANSI/IEEE 1149.1-1993 compliant devices.

Example 5-1. Boundary-Scan Description Language (BSDL) Example (Sheet 1 of 6)

```
-- i960 (R) Hx Processor BSDL Model

-- Rev 0.6      08 Dec  1994
-- The following list describes all of the pins that are contained in the
-- i960 Hx microprocessor.

entity Ha_Processor is
   generic(PHYSICAL_PIN_MAP : string:= “PGA”);

   port (A         : out     bit_vector(2 to 31);
         ADSBAR    : out     bit;
         BEBAR     : out     bit_vector(0 to 3);
         BLASTBAR  : out     bit;
         BOFFBAR   : in      bit;
         BREQ      : out     bit;
         BSTALL    : out     bit;
         BTERMBAR  : in      bit;
         CT        : out     bit_vector(0 to 3);
         CLKIN     : in      bit;
         D         : inout   bit_vector(0 to 31);
         DENBAR    : out     bit;
         DP        : inout   bit_vector(0 to 3);
         DTRBAR    : out     bit;
         DCBAR     : out     bit;
         FAILBAR   : out     bit;
         HOLD      : in      bit;
         HOLDA     : out     bit;
         LOCKBAR   : out     bit;
```

Example 5-1. Boundary-Scan Description Language (BSDL) Example (Sheet 2 of 6)

```
        NMIBAR    : in      bit;
        ONCEBAR   : in      bit;
        PCHKBAR   : out     bit;
        READYBAR  : in      bit;
        RESETBAR  : in      bit;
        STEST     : in      bit;
        SUPBAR    : out     bit;
        TCK       : in      bit;
        TDI       : in      bit;
        TDO       : out     bit;
        TMS       : in      bit;
        TRST      : in      bit;
        WAITBAR   : out     bit;
        WRBAR     : out     bit;
        XINTBAR   : in      bit_vector(0 to 7);
        FIVEVREF  : linkage bit;
        VCCPLL    : linkage bit;
        VOLTDET   : out     bit;
        VCC1      : linkage bit_vector(0 to 23);
        VCC2      : linkage bit_vector(0 to 20);
        VSS1      : linkage bit_vector(0 to 25);
        VSS2      : linkage bit_vector(0 to 22);
        NC        : linkage bit_vector(0 to 4)

);

use STD_1149_1_1990.all;
use i960ha_a.all;


attribute PIN_MAP of Ha_Processor : entity is PHYSICAL_PIN_MAP;



 constant PGA:PIN_MAP_STRING :=

     "A         : (D16, D17, E16, E17, F17, G16, G17, H17, J17, K17,"&
     "             L17, L16, M17, N17, N16, P17, Q17, P16, P15, Q16,"&
     "             R17, R16, Q15, S17, R15, S16, Q14, R14, Q13, S15),"&
     "ADSBAR    : R06,"&
     "BEBAR     : (R09, S07, S06, S05),"&
     "BLASTBAR  : S08,"&
     "BOFFBAR   : B01,"&
     "BREQ      : R13,"&
     "BSTALL    : R12,"&
     "BTERMBAR  : R04,"&
     "CT        : (A11, A12, A13, A14),"&
     "CLKIN     : C13,"&
     "D         : (E03, C02, D02, C01, E02, D01, F02, E01, F01, G01,"&
     "             H02, H01, J01, K01, L02, L01, M01, N01, N02, P01,"&
     "             P02, Q01, P03, Q02, R01, S01, Q03, R02, Q04, S02,"&
     "             Q05, R03),"&
```

Example 5-1. Boundary-Scan Description Language (BSDL) Example (Sheet 3 of 6)

```
        "DENBAR     : S09,"&
        "DP         : (A03, B03, A04, B04),"&
        "DTRBAR     : S11,"&
        "DCBAR      : S13,"&
        "FAILBAR    : A02,"&
        "HOLD       : R05,"&
        "HOLDA      : S04,"&
        "LOCKBAR    : S14,"&
        "NMIBAR     : D15,"&
        "ONCEBAR    : C03,"&
        "PCHKBAR    : B08,"&
        "READYBAR   : S03,"&
        "RESETBAR   : A16,"&
        "STEST      : B02,"&
        "SUPBAR     : Q12,"&
        "TCK        : B05,"&
        "TDI        : A07,"&
        "TDO        : A08,"&
        "TMS        : B06,"&
        "TRST       : A06,"&
        "WAITBAR    : S12,"&
        "WRBAR      : S10,"&
        "XINTBAR    : (B15, A15, A17, B16, C15, B17, C16, C17),"&
        "FIVEVREF   : C05,"&
        "VOLTDET    : A05,"&
        "VCCPLL     : B10,"&
        "VCC1       : (M02, K02, J02, G02, N03, F03, C06, B07, B09, B11,"&
        "             B12, C14, E15, F16, H16, J16, K16, M16, N15, Q06,"&
        "             R07, R08, R10, R11),"&
        "VSS1       : (G03, H03, J03, K03, L03, M03, C07, C08, C09, C10,"&
        "             C11, C12, Q07, Q08, Q09, Q10, Q11, F15, G15, H15,"&
        "             J15, K15, L15, M15, A01, C04),"&
    "NC         : (A09, A10, B13, B14, D03)";


  attribute Tap_Scan_In    of  TDI   : signal is true;
  attribute Tap_Scan_Mode  of  TMS   : signal is true;
  attribute Tap_Scan_Out   of  TDO   : signal is true;
  attribute Tap_Scan_Reset of  TRST  : signal is true;
  attribute Tap_Scan_Clock of  TCK   : signal is (66.0e6, BOTH);

  attribute Instruction_Length of Ha_Processor: entity is 4;

  attribute Instruction_Opcode of Ha_Processor: entity is

     "BYPASS     (1111)," &
     "EXTEST     (0000)," &
     "SAMPLE     (0001)," &
     "IDCODE     (0010)," &
     "RUBIST     (0111)," &
     "Reserved   (1011, 1100)";
```

Example 5-1. Boundary-Scan Description Language (BSDL) Example (Sheet 4 of 6)

```
   attribute Instruction_Capture of Ha_Processor: entity is “0001”;

   attribute Instruction_Private of Ha_Processor: entity is “Reserved” ;

   attribute Idcode_Register of Ha_Processor: entity is
      “0000”                  &  --version,
      “1000100001000000”      &  --part number
      “00000001001”           &  --manufacturers identity
      “1”;                       --required by the standard

   attribute Register_Access of Ha_Processor: entity is
     “Runbist[32]     (RUBIST),” &
     “Bypass          (CLAMP, HIGHZ)”;

--{*********************************************************************}
--{  The first cell, cell 0, is closest to TDO                           }
--{  BC_1:Control, Output3  CBSC_1:Bidir  BC_4: Input, Clock             }
--{*********************************************************************}

   attribute Boundary_Cells of Ha_Processor: entity is “BC_4, BC_1, CBSC_1”;
   attribute Boundary_Length of Ha_Processor: entity is 112;
   attribute Boundary_Register of Ha_Processor: entity is

      “0  (CBSC_1,  DP(3),       bidir,   X,   17, 1,  Z),”   &
      “1  (CBSC_1,  DP(2),       bidir,   X,   17, 1,  Z),”   &
      “2  (CBSC_1,  DP(0),       bidir,   X,   17, 1,  Z),”   &
      “3  (CBSC_1,  DP(1),       bidir,   X,   17, 1,  Z),”   &
      “4  (BC_4,    STEST,       input,   X),”   &
      “5  (BC_1,    FAILBAR,     output3, X,   6,  1,  Z),”   &
      “6  (BC_1,    *,           control, 1),”   &
      “7  (BC_4,    ONCEBAR,     input,   X),”   &
      “8  (BC_4,    BOFFBAR,     input,   X),”   &
      “9  (CBSC_1,  D(0),        bidir,   X,  17,  1,  Z),”   &
      “10 (CBSC_1,  D(1),        bidir,   X,  17,  1,  Z),”   &
      “11 (CBSC_1,  D(2),        bidir,   X,  17,  1,  Z),”   &
      “12 (CBSC_1,  D(3),        bidir,   X,  17,  1,  Z),”   &
      “13 (CBSC_1,  D(4),        bidir,   X,  17,  1,  Z),”   &
      “14 (CBSC_1,  D(5),        bidir,   X,  17,  1,  Z),”   &
      “15 (CBSC_1,  D(6),        bidir,   X,  17,  1,  Z),”   &
      “16 (CBSC_1,  D(7),        bidir,   X,  17,  1,  Z),”   &
      “17 (BC_1,    *,           control, 1),”   &
      “18 (CBSC_1,  D(8),        bidir,   X,  17,  1,  Z),”   &
      “19 (CBSC_1,  D(9),        bidir,   X,  17,  1,  Z),”   &
      “20 (CBSC_1,  D(10),       bidir,   X,  17,  1,  Z),”   &
      “21 (CBSC_1,  D(11),       bidir,   X,  17,  1,  Z),”   &
      “22 (CBSC_1,  D(12),       bidir,   X,  17,  1,  Z),”   &
      “23 (CBSC_1,  D(13),       bidir,   X,  17,  1,  Z),”   &
      “24 (CBSC_1,  D(14),       bidir,   X,  17,  1,  Z),”   &
      “25 (CBSC_1,  D(15),       bidir,   X,  17,  1,  Z),”   &
      “26 (CBSC_1,  D(16),       bidir,   X,  17,  1,  Z),”   &
      “27 (CBSC_1,  D(17),       bidir,   X,  17,  1,  Z),”   &
      “28 (CBSC_1,  D(18),       bidir,   X,  17,  1,  Z),”   &
```

Example 5-1. Boundary-Scan Description Language (BSDL) Example (Sheet 5 of 6)

```
      “29 (CBSC_1,  D(19),       bidir,   X,  17,  1,  Z),”   &
      “30 (CBSC_1,  D(20),       bidir,   X,  17,  1,  Z),”   &
      “31 (CBSC_1,  D(21),       bidir,   X,  17,  1,  Z),”   &
      “32 (CBSC_1,  D(22),       bidir,   X,  17,  1,  Z),”   &
      “33 (CBSC_1,  D(23),       bidir,   X,  17,  1,  Z),”   &
      “34 (CBSC_1,  D(24),       bidir,   X,  17,  1,  Z),”   &
      “35 (CBSC_1,  D(25),       bidir,   X,  17,  1,  Z),”   &
      “36 (CBSC_1,  D(26),       bidir,   X,  17,  1,  Z),”   &
      “37 (CBSC_1,  D(27),       bidir,   X,  17,  1,  Z),”   &
      “38 (CBSC_1,  D(28),       bidir,   X,  17,  1,  Z),”   &
      “39 (CBSC_1,  D(29),       bidir,   X,  17,  1,  Z),”   &
      “40 (CBSC_1,  D(30),       bidir,   X,  17,  1,  Z),”   &
      “41 (CBSC_1,  D(31),       bidir,   X,  17,  1,  Z),”   &
      “42 (BC_4,    BTERMBAR,    input,   X),”   &
      “43 (BC_4,    READYBAR,    input,   X),”   &
      “44 (BC_4,    HOLD,        input,   X),”   &
      “45 (BC_1,    HOLDA,       output3, X,  46, 1,  Z),”   &
      “46 (BC_1,    *,           control, 1),”  &
      “47 (BC_1,    ADSBAR,      output3, X,  61, 1,  Z),”   &
      “48 (BC_1,    BEBAR(3),    output3, X,  61, 1,  Z),”   &
      “49 (BC_1,    BEBAR(2),    output3, X,  61, 1,  Z),”   &
      “50 (BC_1,    BEBAR(1),    output3, X,  61, 1,  Z),”   &
      “51 (BC_1,    BEBAR(0),    output3, X,  61, 1,  Z),”   &
      “52 (BC_1,    BLASTBAR,    output3, X,  61, 1,  Z),”   &
      “53 (BC_1,    DENBAR,      output3, X,  61, 1,  Z),”   &
      “54 (BC_1,    WRBAR,       output3, X,  61, 1,  Z),”   &
      “55 (BC_1,    DTRBAR,      output3, X,  56, 1,  Z),”   &
      “56 (BC_1,    *,           control, 1),”  &
      “57 (BC_1,    WAITBAR,     output3, X,  61, 1,  Z),”   &
      “58 (BC_1,    BSTALL,      output3, X,  6,  1,  Z),”   &
      “59 (BC_1,    DCBAR,       output3, X,  61, 1,  Z),”   &
      “60 (BC_1,    SUPBAR,      output3, X,  61, 1,  Z),”   &
      “61 (BC_1,    *,           control, 1),”  &
      “62 (BC_1,    LOCKBAR,     output3, X,  61, 1,  Z),”   &
      “63 (BC_1,    BREQ,        output3, X,  6,  1,  Z),”   &
      “64 (BC_1,    A(31),       output3, X,  80, 1,  Z),”   &
      “65 (BC_1,    A(30),       output3, X,  80, 1,  Z),”  &
      “66 (BC_1,    A(29),       output3, X,  80, 1,  Z),”  &
      “67 (BC_1,    A(28),       output3, X,  80, 1,  Z),”  &
      “68 (BC_1,    A(27),       output3, X,  80, 1,  Z),”   &
      “69 (BC_1,    A(26),       output3,  X,  80, 1,  Z),”   &
      “70 (BC_1,    A(25),       output3,  X,  80, 1,  Z),”   &
      “71 (BC_1,    A(24),       output3,  X,  80, 1,  Z),”   &
      “72 (BC_1,    A(23),       output3,  X,  80, 1,  Z),”   &
      “73 (BC_1,    A(22),       output3,  X,  80, 1,  Z),”   &
      “74 (BC_1,    A(21),       output3,  X,  80, 1,  Z),”   &
      “75 (BC_1,    A(20),       output3,  X,  80, 1,  Z),”   &
      “76 (BC_1,    A(19),       output3,  X,  80, 1,  Z),”   &
      “77 (BC_1,    A(18),       output3,  X,  80, 1,  Z),”   &
      “78 (BC_1,    A(17),       output3,  X,  80, 1,  Z),”   &
      “79 (BC_1,    A(16),       output3,  X,  80, 1,  Z),”   &
      “80 (BC_1,    *,           control,  1),”   &
```

Example 5-1. Boundary-Scan Description Language (BSDL) Example (Sheet 6 of 6)

```
      “81 (BC_1,    A(15),       output3,  X,  80, 1,  Z),”   &
      “82 (BC_1,    A(14),       output3,  X,  80, 1,  Z),”   &
      “83 (BC_1,    A(13),       output3,  X,  80, 1,  Z),”   &
      “84 (BC_1,    A(12),       output3,  X,  80, 1,  Z),”   &
      “85 (BC_1,    A(11),       output3,  X,  80, 1,  Z),”   &
      “86 (BC_1,    A(10),       output3,  X,  80, 1,  Z),”   &
      “87 (BC_1,    A(9),        output3,  X,  80, 1,  Z),”   &
      “88 (BC_1,    A(8),        output3,  X,  80, 1,  Z),”   &
      “89 (BC_1,    A(7),        output3,  X,  80, 1,  Z),”   &
      “90 (BC_1,    A(6),        output3,  X,  80, 1,  Z),”   &
      “91 (BC_1,    A(5),        output3,  X,  80, 1,  Z),”   &
      “92 (BC_1,    A(4),        output3,  X,  80, 1,  Z),”   &
      “93 (BC_1,    A(3),        output3,  X,  80, 1,  Z),”   &
      “94 (BC_1,    A(2),        output3,  X,  80, 1,  Z),”   &
      “95 (BC_4,    NMIBAR,      input,    X),”   &
      “96 (BC_4,    XINTBAR(7),  input,    X),”   &
      “97 (BC_4,    XINTBAR(6),  input,    X),”   &
      “98 (BC_4,    XINTBAR(5),  input,    X),”   &
      “99 (BC_4,    XINTBAR(4),  input,    X),”   &
      “100(BC_4,    XINTBAR(3),  input,    X),”   &
      “101(BC_4,    XINTBAR(2),  input,    X),”   &
      “102(BC_4,    XINTBAR(1),  input,    X),”   &
      “103(BC_4,    XINTBAR(0),  input,    X),”   &
      “104(BC_4,    RESETBAR,    input,    X),”   &
      “105(BC_4,    CLKIN,       input,    X),”   &
      “106(BC_1,    CT(3),       output3,  X,   80, 1, Z),”   &
      “107(BC_1,    CT(2),       output3,  X,   80, 1, Z),”   &
      “108(BC_1,    CT(1),       output3,  X,   80, 1, Z),”   &
      “109(BC_1,    CT(0),       output3,  X,   80, 1, Z),”   &
      “110(BC_1,    PCHKBAR,     output3,  X,  111, 1, Z),”   &
      “111(BC_1,    *,           control,  1)”;
end Ha_Processor;
```

Table 24. Data Sheet Version -002 to -003 Revision History

Section	Description
Table 19, DC Characteristics (pg. 29) Table 20, 80960Hx AC Characteristics (pg. 30)	Added 3V and 5V AC and DC specifications based on design simulations.
Table 6, 80960Hx Processor Family Pin Descriptions (pg. 6)	HOLDA pin definition during BOFF mode corrected. Added text indicating that the $\overline{\text{TRST}}$ pin must be reset after power-up, just like $\overline{\text{RESET}}$.
Table 9, 80960Hx PQ2 Pinout — Signal Name Order (pg. 18) Table 10, 80960Hx PQ2 Pinout — Pin Number Order (pg. 20)	New tables.
Table 12, 80960Hx 168-Pin PGA Package Thermal Characteristics (pg. 23) Table 11, Maximum TA at Various Airflows in oC (PGA Package Only) (pg. 23)	Added thermal data for PGA and PQ2 packages.
Figure 6, 80960Hx Device Identification Register (pg. 25)	Added device ID for 80960HT
Figure 24, Output Delay or Hold vs. Load Capacitance (pg. 39)	New figure.
Example 5-1, Boundary-Scan Description Language (BSDL) Example (pg. 73)	New Example.